Unclassified

SECURITY CLASSIFICATION OF THIS PAGE

REPORT DOCUMENTATION PAGE

1a. REPORT SECURITY CLASSIFICATION: Unclassified	1b. RESTRICTIVE MARKINGS
2a. SECURITY CLASSIFICATION AUTHORITY	3. DISTRIBUTION/AVAILABILITY OF REPORT: Approved for public release, distribution unlimited
2b. DECLASSIFICATION/DOWNGRADING SCHEDULE	
4. PERFORMING ORGANIZATION REPORT NUMBER(S)	5. MONITORING ORGANIZATION REPORT NUMBER(S): AFOSR-TR- 88-0834
6a. NAME OF PERFORMING ORGANIZATION: GTE Laboratories Incorporated; 6b. OFFICE SYMBOL (If applicable): 24577	7a. NAME OF MONITORING ORGANIZATION: AFOSR/NP
6c. ADDRESS (City, State and ZIP Code): 40 Sylvan Road, Waltham, MA 02254	7b. ADDRESS (City, State and ZIP Code): Bolling AFB DC 20332-6448 BLG 410
8a. NAME OF FUNDING/SPONSORING ORGANIZATION: Air Force Office of Scientific Research; 8b. OFFICE SYMBOL (If applicable): NP	9. PROCUREMENT INSTRUMENT IDENTIFICATION NUMBER: F49620-86-C-0034
8c. ADDRESS (City, State and ZIP Code): Bolling AFB DC 20332-6448 BLG 410	10. SOURCE OF FUNDING NOS.

PROGRAM ELEMENT NO.	PROJECT NO.	TASK NO.	WORK UNIT NO.
61102F	2301	A7	

11. TITLE (Include Security Classification): Transport and Junction Physics in Semiconductor-Metal Eutectic Composites (U)

12. PERSONAL AUTHOR(S): B. Ditchek, J. Gustafson

13a. TYPE OF REPORT	13b. TIME COVERED	14. DATE OF REPORT (Yr., Mo., Day)	15. PAGE COUNT
Final Report	FROM 4/1/86 TO 3/31/88	1988 May 31	121

16. SUPPLEMENTARY NOTATION

17. COSATI CODES			18. SUBJECT TERMS (Continue on reverse if necessary and identify by block number)
FIELD	GROUP	SUB. GR.	Solid State Switching; Electron Beam Induced Current; Eutectic Composites; Depletion Zones; (jhd)

19. ABSTRACT (Continue on reverse if necessary and identify by block number)

An investigation of the transport and junction physics of Si-$TaSi_2$ semiconductor-metal eutectic composites has demonstrated the potential use of this class of materials in high-power switching. Following the development of single-crystal matrix Si-$TaSi_2$ crystals, eutectic diodes utilizing the in situ junctions were fabricated and analyzed using current-voltage, capacitance-voltage, and electron-beam-induced current techniques. Studies demonstrated nearly ideal diode behavior, a Schottky barrier height of 0.62 eV, and a means of measuring the extent of the depletion zones and the carrier concentration of the semiconductor matrix. An analysis based on a comparison of the EBIC-determined carrier concentration with the Hall carrier concentration resulted in a measure of the effect of the depletion zones on composite resistivity. Building on the foundation provided by this analysis, the first eutectic composite transistors were demonstrated. These devices confirmed that current flow can be controlled by "pinching-off" Si channels between $TaSi_2$ rods. Furthermore, testing at high voltages indicated that the eutectic devices are resistant to avalanche breakdown. Devices have been built that block 600 V, three times

20. DISTRIBUTION/AVAILABILITY OF ABSTRACT	21. ABSTRACT SECURITY CLASSIFICATION
UNCLASSIFIED/UNLIMITED ☒ SAME AS RPT ☒ DTIC USERS ☐	Unclassified

22a. NAME OF RESPONSIBLE INDIVIDUAL	22b. TELEPHONE NUMBER	22c. OFFICE SYMBOL
Lt Col Bruce L. Smith	202-767-4908	NP

DD FORM 1473, 83 APR EDITION OF 1 JAN 73 IS OBSOLETE.

Unclassified

SECURITY CLASSIFICATION OF THIS PAGE

the value for a conventional planar device in a wafer of the same carrier concentration. Analysis of these devices has indicated that much higher blocking voltages can be achieved by simply increasing the gate-to-drain distance to avoid a "punch-through-related" voltage limitation. The study suggests that scaling up device dimensions may enable the switching of the very large currents and voltages of interest for pulsed power applications.

ABSTRACT

An investigation of the transport and junction physics of Si-$TaSi_2$ semiconductor-metal eutectic composites has demonstrated the potential use of this class of materials in high-power switching. Following the development of single-crystal matrix Si-$TaSi_2$ crystals, eutectic diodes utilizing the *in situ* junctions were fabricated and analyzed using current-voltage, capacitance-voltage, and electron-beam-induced current techniques. Studies demonstrated nearly ideal diode behavior, a Schottky barrier height of 0.62 eV, and a means of measuring the extent of the depletion zones and the carrier concentration of the semiconductor matrix. An analysis based on a comparison of the EBIC-determined carrier concentration with the Hall carrier concentration resulted in a measure of the effect of the depletion zones on composite resistivity. Building on the foundation provided by this analysis, the first eutectic composite transistors were demonstrated. These devices confirmed that current flow can be controlled by "pinching-off" Si channels between $TaSi_2$ rods. Furthermore, testing at high voltages indicated that the eutectic devices are resistant to avalanche breakdown. Devices have been built that block 600 V, three times the value for a conventional planar device in a wafer of the same carrier concentration. Analysis of these devices has indicated that much higher blocking voltages can be achieved by simply increasing the gate-to-drain distance to avoid a "punch-through-related" voltage limitation. The study suggests that scaling up device dimensions may enable the switching of the very large currents and voltages of interest for pulsed power applications.

TABLE OF CONTENTS

TABLE OF CONTENTS (Continued)

LIST OF FIGURES

LIST OF FIGURES (Continued)

1. INTRODUCTION

Semiconductor-metal eutectic (SME) composites, composed of an array of metallic rods distributed throughout a semiconductor matrix and formed directly by directional solidification of a eutectic mixture, represent a new class of electronic materials with the potential to enhance and expand the capabilities of high-power, solid state switching technology. The objective of this two-year program was to perform basic research on the electrical transport and junction properties of these novel materials to enable an evaluation of their high-power device potential.

SME materials are two-phase composite materials and differ from the single-phase materials that have always been used to create electronic devices in the past. Although composites have been successfully applied as structural materials, they have never before been used as devices providing electronic control. Previous tenets of semiconductor device physics required that the active semiconductor material be free of any second phase. Clearly, metallic inclusions would lead to high leakage currents and low-voltage breakdown. Thus, the development and application of SME composite materials for high- voltage operation deviates significantly from conventional approaches to forming high-voltage devices.

Rapid progress has been made in the growth, characterization, and device physics of these novel materials. Prior to the start of this program, the state of the art was represented by the Si-$TaSi_2$ SME with polycrystalline matrices having a carrier concentration low enough to satisfy the criterion for "pinching-off" the flow of current between adjacent $TaSi_2$ rods by the application of a gate bias voltage. At the close of this two-year program, high-voltage transistors have been demonstrated in quasi-single- crystalline Si-$TaSi_2$ composites. These initial devices have demonstrated not only the feasibility of using this unique two-phase equilibrium structure to switch currents, but also the fact that SME devices excel at high voltage applications and are resistant to avalanche breakdown, the failure mechanism that limits the blocking voltage of conventional devices.

In addition, the program has developed an understanding of the special "grown-in" metal-semiconductor Schottky junctions inherent to these materials and the dependence of the composite conductivity on the cylindrical depletion zones surrounding the rods. The data and insight provided by these fundamental studies were crucial to the successful demonstration of transistor action in SME composites and will be equally essential to the continued development of these materials for high-power and other electronic device applications.

In this report, the growth of the composite Si-$TaSi_2$ is discussed in Section 2. Studies of the Si-$NbSi_2$ eutectic composite are also discussed. Section 3 covers the properties of the Si-$TaSi_2$ eutectic junction and includes the method for making contacts as well as current-voltage (I-V), capacitance-voltage (C-V), and electron-beam-induced current (EBIC) analyses. The transport properties of the composites, particularly the effect of the depletion zones on the composite resistivity, are discussed in Section 4. The development of the eutectic composite transistor, interpretation of the characteristics in terms of junction properties and depletion zone limited transport, and evidence for the device's resistance to avalanche breakdown are presented in Section 5. Additional data relevant to the evaluation of the composite device for high-power operation but not derived at under this contract are included in Section 6. Finally, an analysis of the device potential for pulsed power operation and recommendations for future study are presented in Section 7. The Appendix is composed of reprints and preprints of publications supported by this contract.

2. EUTECTIC COMPOSITE MATERIALS

The directional solidification of the Si-$TaSi_2$ eutectic composite yields a material with a rod-like distribution of the $TaSi_2$ phase in a Si matrix. The eutectic composition corresponds to about 2 v/o $TaSi_2$. The scale of the eutectic microstructure is determined by the growth rate, such that $\lambda^2 v = 1.25 \times 10^{-5}$ cm^3/h, where λ is the average interrod spacing and v is the growth rate. During the course of these experiments all boules were grown at 20 cm/h to yield, according to the above relation, an average interrod spacing of 7.9 μm. Because of the importance of rod density on device properties, the rod density was measured for all boules studied. Where possible the measurements were made in the region of devices used for determination of other properties, such as carrier concentration. Measurements of the rod density varied between 1.4 and 2.2 ($\times 10^6$) rods/cm^2.

The growth technique employed is called Czochralski crystal pulling and is analogous to the most common technique for growing large Si crystals for the electronics industry. After the melting of a charge of the eutectic composition a Si seed is lowered onto the melt surface, given time to thermally equilibrate, and then pulled up at the fixed rate of 20 cm/h. The composite boule solidifies as the seed is pulled. This process of directional solidification yields the eutectic rod-like microstructure with the rods oriented along the growth direction.

Initially, the boules grown had polycrystalline Si matrices. Fabrication of devices on these substrates always led to excessive leakage and nearly ohmic, nonrectifying behavior. It was found, however, that composites with a single-crystal Si matrix could be obtained using certain techniques. Growth of a single-crystal matrix eutectic depends primarily on using the exact eutectic composition and minimizing certain impurities. Due to loss of Si as SiO and the meltback of a fraction of the seed, maintaining the eutectic composition can be difficult. Nevertheless, proper balancing of the two effects can be achieved, and over 20 single-crystal matrix boules with a (111) Si matrix have been grown over the course of this program. Typical boules weighed 50 to 100 grams and had a 0.5 in. to 1 in. diameter. A photograph of a typical single-crystal matrix (111) boule is shown in Figure 1.

A typical transverse section microstructure of the Si-$TaSi_2$ eutectic is shown in Figure 2. The figure shows that rods in the eutectic are neither arranged in a regular lattice-like array nor distributed in a strictly random pattern. Examination of many such sections has revealed a kind of cellular structure. The interrod spacing in the cell walls is less than the average interrod spacing. For the case of λ = 7.9 μm, the rods in the cell walls have an average interrod spacing of only 4.5 μm. The interior of the cells exhibits a very low rod density and covers an area with a diameter several times the average

interrod spacing. The cellular nature of the rod distribution will be shown to be important in analyzing the effect of depletion zones on transport in these composites.

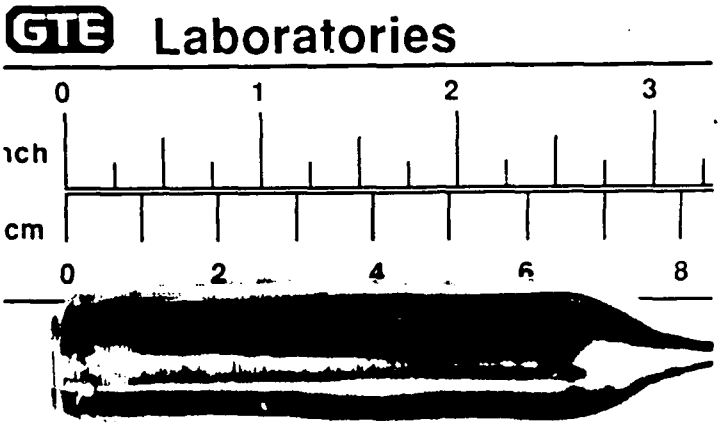


Figure 1. Photograph of a typical single-crystal (111) matrix Si-$TaSi_2$ eutectic composite.

Examination of longitudinal sections of the boule also indicates that the rods are not all perfectly aligned and that some divergence of the rods relative to the wafer normal may exist. Using the EBIC technique discussed in Section 3.3, the maximum divergence of the rods has been measured to be 6 degrees. Rod misalignment has been shown to be a microstructural factor adversely affecting switch performance (Section 5.3).

Due to the need for an n-type Si matrix, the Si used in the charge was always lightly doped with P. As will be shown in the following section, carrier concentrations in the Si matrix were later determined to be in the low 10^{15} cm^{-3} range, about a factor of two higher than the P concentration of the charge. The additional P probably originates as an impurity in the 99.996 % pure Ta used. Nevertheless, the P does segregate as expected based on its segregation coefficient of about 0.35 for Si.

The Si-$NbSi_2$ eutectic has also been examined. This eutectic contains 2.8 v/o silicide in a matrix of Si. The growth rate for this system is given by $\lambda^2 v = 1.05 \times 10^{-5}$ cm^3/h, just slightly less than the value for the Si-$TaSi_2$ eutectic. The microstructure of this eutectic, however, always tended to be more irregular than the benchmark Si-$TaSi_2$. Probably as a result of the added irregularity, single-crystal matrix growth was much more difficult to achieve. Since the anticipated advantages over the Si-$TaSi_2$ system were considered small, additional work on this system was discontinued.

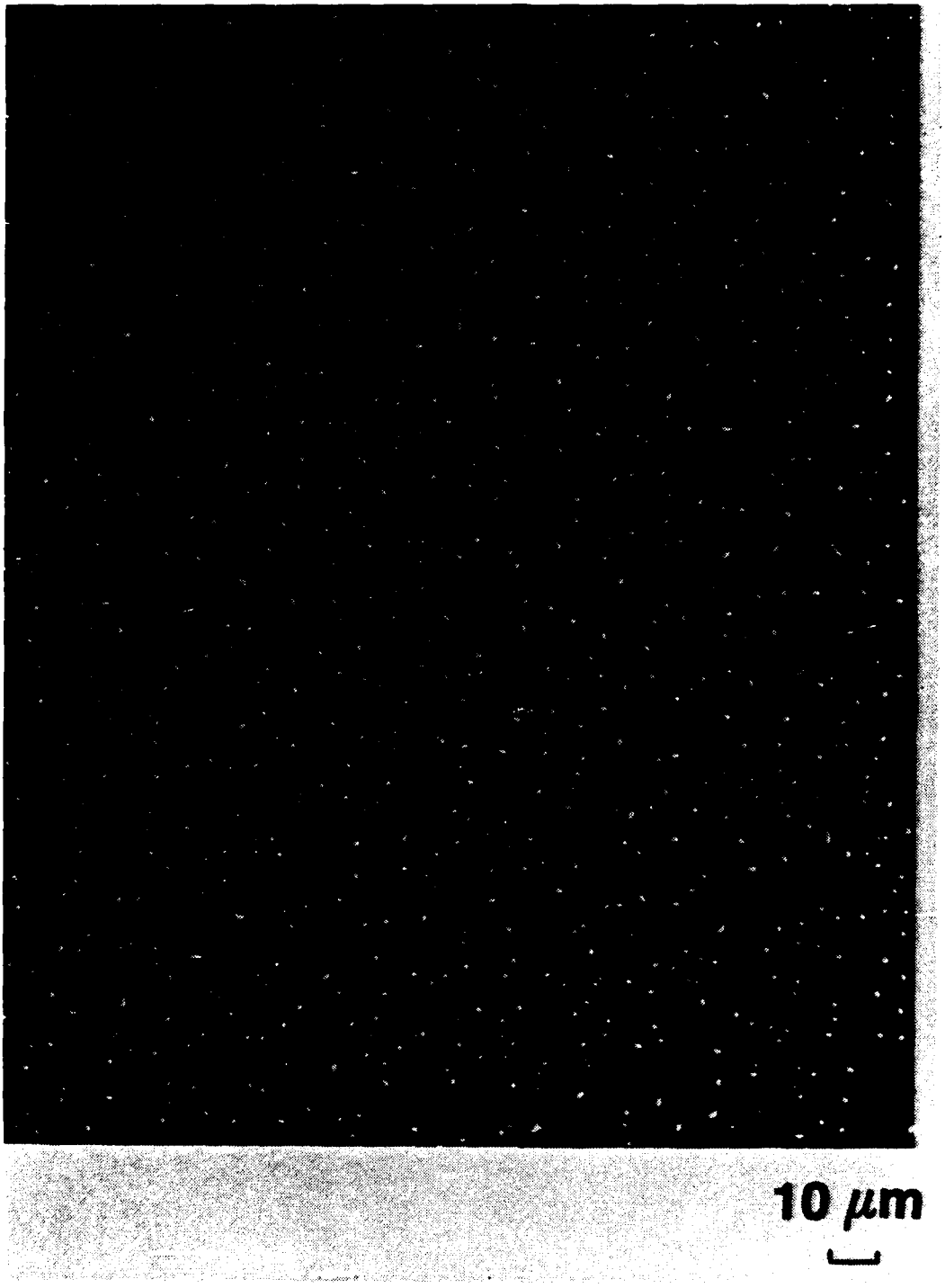


Figure 2. A transverse section of a Si-$TaSi_2$ eutectic composite. Note the cellular arrangement of the $TaSi_2$ rods.

3. PROPERTIES OF THE Si-$TaSi_2$ EUTECTIC JUNCTION

3.1 EUTECTIC DIODE RELATIONS

The $TaSi_2$ phase in the eutectic composite is approximately cylindrical. Consequently, analysis of the Schottky junctions surrounding the rods cannot be performed with application of the usual planar junction equations. The analysis must account for the geometrical difference between a cylindrical and a planar junction. The spatially varying potential at the Schottky junction between a semiconductor and a metal is given by Poisson's equation (for reference in this section see, for example, Ref. 1),

$$\nabla^2 V = -q N_d/\varepsilon_s, \tag{1}$$

where V is the potential, q is the unit charge, N_d is the donor concentration, and ε_s is the dielectric constant. The solution using cylindrical coordinates with a rod radius of r_o and boundary conditions

$$(\partial V/\partial r) = 0 \qquad \text{when} \quad r = r_o + W \tag{2}$$

and

$$V = - V_b \qquad \text{when} \quad r = r_o \tag{3}$$

yields

$$[\,(r_o + W)^2 - r_o^2 - 2(r_o + W)^2 \ln((r_o + W)/r_o)\,] = -(4\varepsilon_s/qN_d)(V_b + V_r), \tag{4}$$

where W is the depletion zone width, V_b is φ_b/q (φ_b is the Schottky barrier height), and V_r is the applied reverse bias voltage of the diode. Equation 4 describes the relationship between the depletion zone width and the reverse bias voltage of a diode. For a given reverse bias voltage, the depletion zone width is smaller and the electric field is more concentrated for a cylindrical junction than it is for a planar junction.

Analysis of eutectic diodes has been performed using current-voltage (I-V), capacitance-voltage (C-V), and electron-beam-induced current (EBIC) techniques. Interpretation of the I-V characteristics may be based on the same thermionic emission diode equation used for planar junctions. In this case,

$$I = A_j A^* T^2 \exp(-q\varphi_b/kT)[\exp(qV/kT)-1], \quad (5)$$

where A_j is the junction area, A* is the Richardson constant equal to 120 A/cm K, and n is the ideality factor characterizing the diode. For an ideal diode n = 1.0.

Analysis of the junction capacitance requires treating the cylindrical junctions like coaxial capacitors. For a parallel set of N_r coaxial capacitors of inner and outer radii, r_o and $(r_o + W)$,

$$C = (2\pi\varepsilon_s l N_r) / \ln[(r_o + W)/r_o]. \quad (6)$$

The length of the cylinder is l, in this case, assumed equal to the wafer thickness. Thus substituting the value of W for a given V_r yields the C-V_r relation for interpretation of the capacitance-voltage measurement. For a planar junction the C-V_r relation is such that plotting $(1/C^2)$ vs V_r yields a straight line and extrapolating the line to infinite C yields V_b. In the cylindrical junction case, the capacitance decreases more slowly with an increase in V_r than it does for the planar junction.

The electron-beam-induced current technique has also been applied to analysis of the junctions. This technique allows imaging of the depletion zones around the rods and a determination of the dependence of the depletion zone width-reverse bias voltage, W-V_r, for the actual Si-$TaSi_2$ composite structure. As discussed in Section 3.3, this analysis allowed verification of the functional W-V_r dependence as given in Eq. 4 and provided a means for measuring N_d, the donor concentration of the Si matrix surrounding the rods.

3.2 CONTACT FORMATION TECHNIQUES

Fabrication of electronic Si-$TaSi_2$ eutectic devices requires the formation of ohmic and Schottky contacts. The ohmic contacts are readily fabricated by any technique that will provide a metal/n^+ surface layer. Primarily we have adopted a simple evaporation technique. Au-Sb wire is evaporated onto the substrate section requiring the ohmic contact. The wafer is then annealed above the Au-Si eutectic temperature, at 400°C for 1 hr. This forms a reacted Au-Si layer with an Sb-doped n^+ layer at the junction of this film and the underlying Si. Since the eutectic film is irregular and discontinuous in most cases, it is necessary to evaporate an additional metallic layer, usually another Au-film on top of the reacted film.

Because these Au-Sb contacts are readily scratched, the development of a more robust, uniform contact was desired. Experiments were made using a $CoSi_2/n^+$ film to provide the ohmic contact.

For this contact, 800 A of Co was first evaporated by e-beam methods onto the substrate. Silicidation was performed in a rapid thermal annealer (RTA) at 800°C for 12 s. To form the n^+ contact at the silicide/Si junction, As was implanted at 100 kV with a flux of 10^{14} cm^{-2}. Movement of the As from the surface of the silicide film to the junction was performed with another RTA at 800°C to 900°C for 10 s. This technique also worked well to provide the necessary ohmic contact.

The necessary Schottky contacts are grown into the composite, of course, but contact to the desired group of rods must be made without creating additional current leakage paths. The best approach would be to contact the $TaSi_2$ rods without contacting the Si. This proved to be very difficult to perform reliably. The best alternative was to contact the rods with a film that also formed a Schottky barrier with the Si surface in between the rods. It was reasoned that as long as the Schottky barrier of the metallic film with the Si exceeded the Schottky barrier of the *in situ* junctions and the area of the surface Si contact was small relative to the $TaSi_2$/Si junction area, the effect of this junction on diode currents or capacitance would be small.

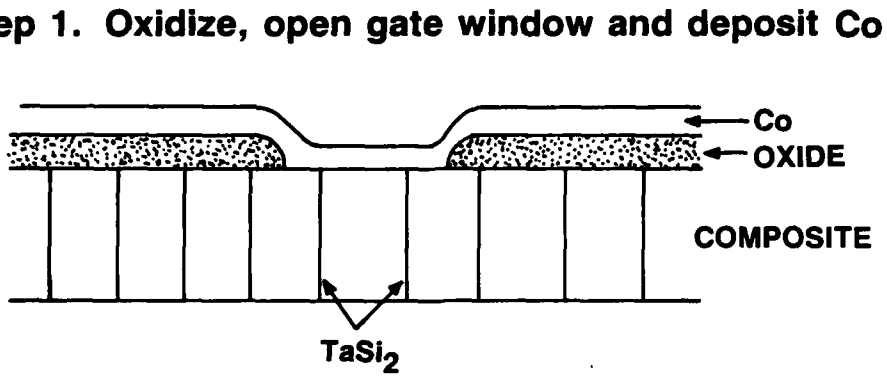
For this purpose three different types of metallic films were examined: evaporated Al, chemical vapor deposited (CVD) W, and $CoSi_2$. The Al contacts yielded nearly ohmic behavior and, consequently, were not pursued further. The best diodes with the W films yielded better results than the Al films but were still leaky. The best W film with a surface contact area of 1.27×10^{-4} cm^2 yielded diode currents of several mA at –10 V. This is considerably above ideal behavior and much higher than the results obtained with the $CoSi_2$ films.

The $CoSi_2$ films were formed as described above for the ohmic contacts but without the implantation and anneal steps. The sequence used, including use of a thermal oxide for developing a self-aligned silicidation process to lithographically form the diode contacts, is shown in Figure 3.

As will be seen in the following section, the $CoSi_2$ films yielded nearly ideal diode behavior. In the 500 μm thick wafers using the diode contact area discussed above, the $TaSi_2$ junction area was 30 to 40 times larger than the surface $CoSi_2$/Si junction area. In addition, the $CoSi_2$/Si Schottky barrier is 0.64 eV, slightly higher than the value obtained for the *in situ* junctions.

The reason for the progression from high leakage currents to low leakage currents as the contact material changed from the Al to W and finally $CoSi_2$ is probably related to the cleanliness and perfection of the Si surface. Al was evaporated without reaction to the Si, hence, the native oxide and near-surface defects and contaminants remained and may have adversely affected the diode properties. The W film deposition technique does cause removal of the native oxide but does not

consume more than 100 A of surface Si. Formation of 2000 A of $CoSi_2$, however, consumes approximately 2000 A of the Si surface yielding a relatively clean, damage-free surface to contact. This probably accounts for the success of this diode contact procedure.



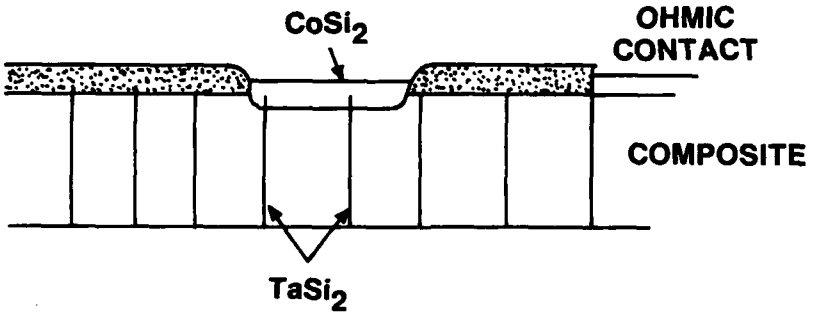


Figure 3. Schematic illustrating the method used to form the surface $CoSi_2$ gate contact film.

3.3 EUTECTIC DIODE PROPERTIES

The I-V characteristics of a typical diode is shown in Figure 4. According to Eq. 1, a plot of ln I vs V should yield a straight line at small voltages with the intercept at 0 V depending on the Schottky barrier height. Figure 5 shows that the linear portion of the forward characteristics extrapolates to 10^{-6} A. Taking the area of the junction as that determined by the 190 one micron diameter, 500 μm length cylindrical rods yields a Schottky barrier height of 0.62 eV, a value very close to the 0.59 eV value determined for planar junctions formed by solid state diffusion of Ta and Si. The diode is well behaved, with an ideality factor n = 1.10 ± 0.05. Deviation from the straight line forward characteristic is determined by the series resistance of the diode. It should be noted that the reverse

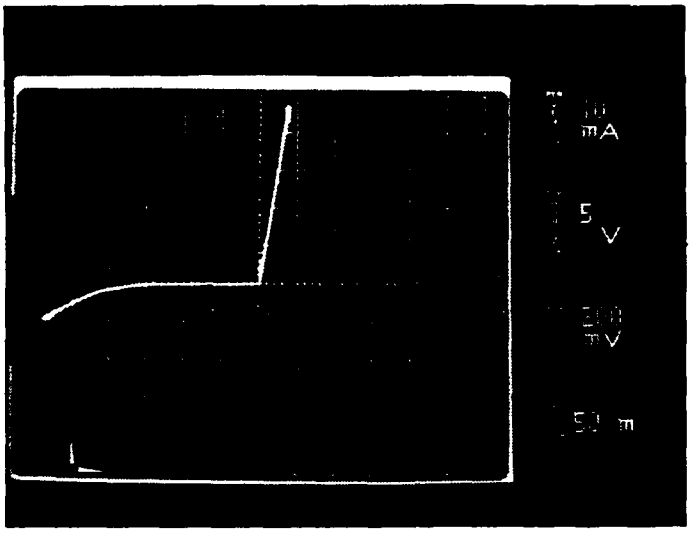


Figure 4. The current-voltage characteristics of a Si-$TaSi_2$ eutectic diode.

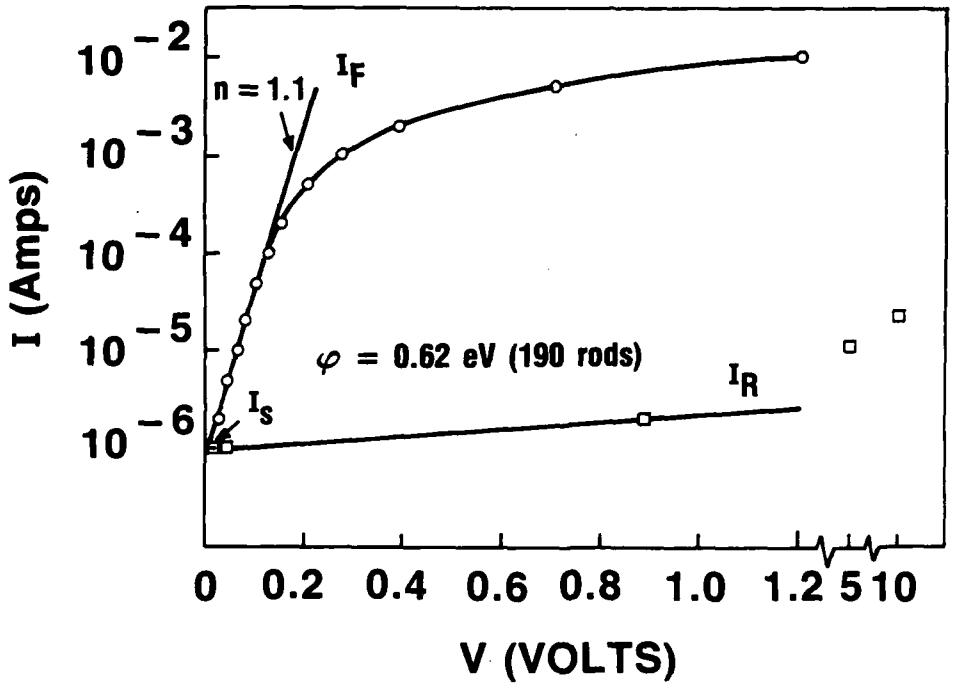


Figure 5. Analysis of the current-voltage characteristics of a Si-$TaSi_2$ eutectic diode. The diode is nearly ideal.

current is also of the order of 10^{-6} A and does not increase significantly until voltages exceed about 5 V. Factors affecting leakage at higher voltage will be discussed further in Section 3.4.

An analysis of the C-V data for a typical diode is shown in Figure 6. The results are presented in the same plot used for analysis of planar junctions. The two solid lines on the graph represent, as denoted, the theoretical C-V dependence for a planar junction and a cylindrical junction. For both lines it is assumed that r_o is 0.6 μm, l = 500 μm, the junction area is the same as that corresponding to the 190 rods, and $N_d = 1.6 \times 10^{15}$ cm^{-3}. The value of the carrier concentration was taken from the Hall effect and may have been an underestimated by about 50%. Nevertheless, the agreement with the cylindrical junction model is quite good, particularly at low voltages. Due to overlap of depletion zones around neighboring rods at higher voltages, the capacitance is lower than predicted by this simple model. Both the I-V and C-V measurements indicate that all the rods under the gate contact are indeed contacted by the surface silicide film and are active parts of the diode.

Application of the EBIC technique has provided additional characterization of the junction. The EBIC technique, performed in the scanning electron microscope (SEM), yields an image of the composite based on the difference in the short-circuit current induced in the diode by the SEM's electron beam as the sample surface is scanned. In the EBIC image, the depletion zones appear bright because the induced current is the greatest in the depletion zone where the electric field is large. Consequently, as shown in the EBIC image in Figure 7, a bright halo around the rods outlines the depletion zone. When the beam is on the $TaSi_2$, no electron-hole pairs are created, and, hence, the position of the rods are marked by dark regions. Using these images, the size of the depletion zones as a function of applied bias voltage was measured. Fitting the results to Eq. 4 determines N_d, the carrier concentration of the semiconductor matrix. For diodes on two different wafers, measurements of W vs V_r are shown in Figure 8, along with calculated values for different concentrations. The actual Si matrix carrier concentration of the two different diodes is readily apparent from this analysis. Also, the similarity of the experimental and the theoretical functional dependence of W on V_r indicates that the phosphorus dopant concentration in the matrix must be uniformly distributed. There is no evidence of the expected P segregation at the $TaSi_2$/Si boundary. Further support for the EBIC carrier concentration method came in its' application to analysis of the P segregation during growth. Using the EBIC technique to convert Hall carrier concentrations to actual carrier concentrations, the segregation coefficient of P in the eutectic boules was measured to be between 0.3 and 0.5, in agreement with the classical value for P in Si of 0.35. Using the uncorrected Hall carrier concentrations, segregation analysis was not possible.

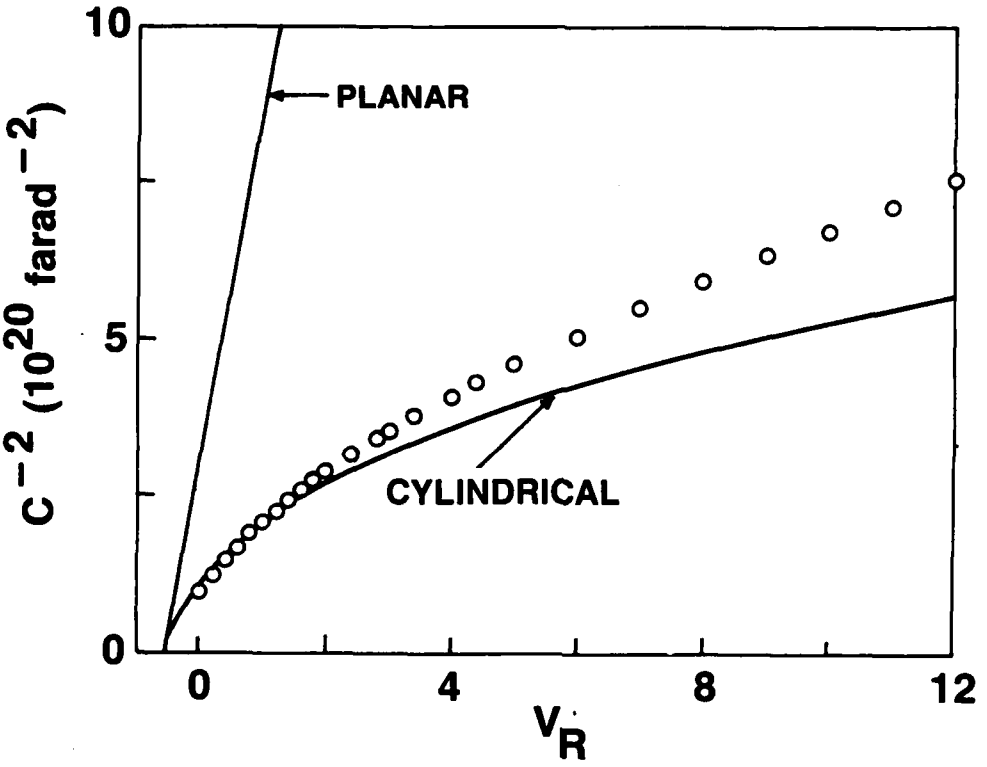


Figure 6. The capacitance-voltage characteristics of a Si-$TaSi_2$ eutectic diode. The data is in accord with the results expected for the specific array of coaxial capacitors under the $CoSi_2$ contact.

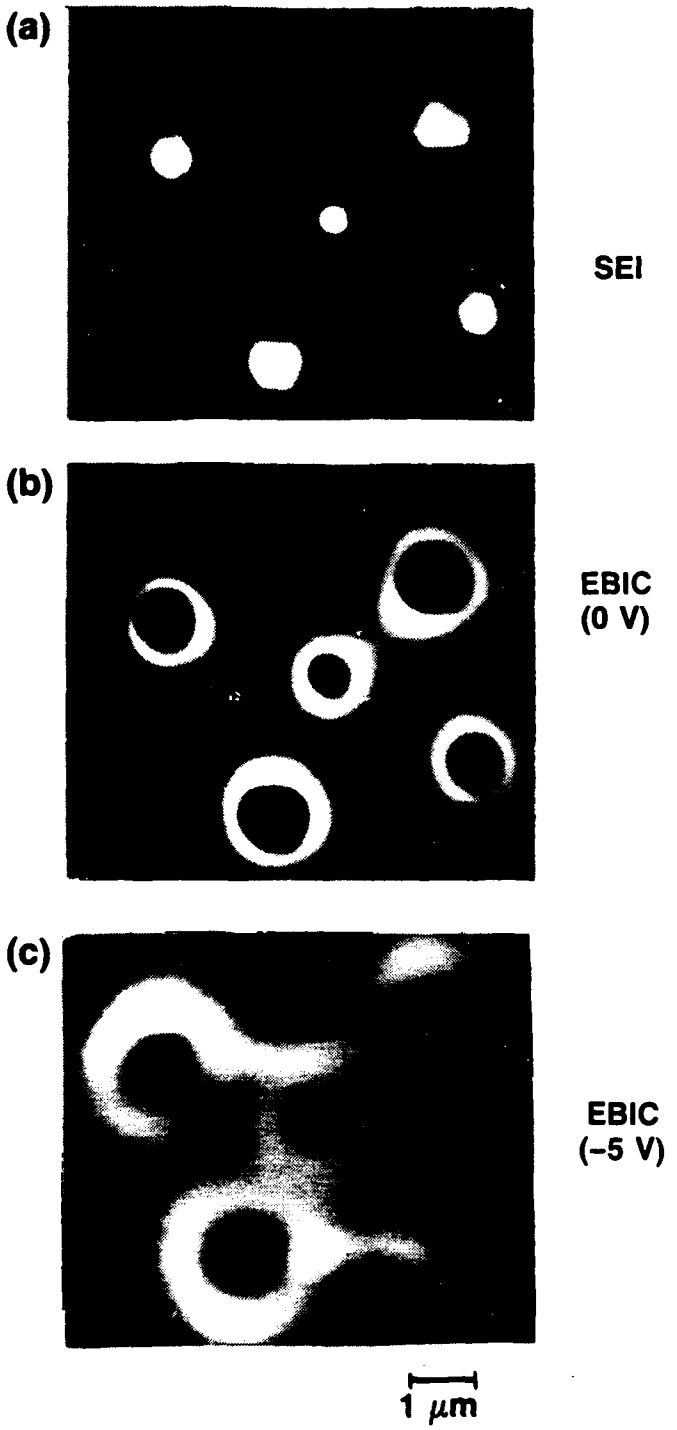


Figure 7. Electron-beam-induced current images of a portion of a Si-$TaSi_2$ eutectic diode. The figure shows five rods in a) secondary electron imaging (SEI) mode, b) EBIC mode without a bias voltage, and c) EBIC mode with a –5 V bias. Note the increase in the size of the depletion zone as the bias voltage is increased.

3.4 DIODES AT HIGH REVERSE BIAS VOLTAGE

According to Eq. 5, the reverse current of a Schottky diode is independent of reverse bias voltage and should never exceed I_s. This is, of course, not the case, and reverse leakage currents increase with bias voltage. Theoretically, two reasons have been proposed for the bias voltage dependence of the reverse diode current ; an image force correction, also called the Schottky effect, and an intrinsic dependence of the barrier height on electric field. This second effect has been empirically demonstrated on $ZrSi_2$/Si junctions. Combining the two effects, Andrews and Lepselter[2] account for increasing reverse currents using Eq. 5 but substituting

$$\varphi_b = \varphi_b^{\circ} - (qE_m/4\pi\varepsilon_s)1/2 - \alpha E_m \qquad (7)$$

for the Schottky barrier height, where E_m is the maximum field at the junction. Andrews and Lepselter found α to be about 1.5×10^{-7}cm. With an intrinsic Shottky barrier height of about 0.6 eV, these effects can cause as much as a factor of 10 increase in current beyond I_s before device breakdown.

At sufficiently high voltage, diodes break down by avalanche effects.[1] When the field at the junction reaches a critical value, electrons overcoming the barrier and contributing to I_s gain sufficient energy to cause electron-hole generation by impact ionization. This multiplication of carriers causes an avalanche of current carriers, and the device breaks down. This is the ultimate voltage limit for all semiconductor devices.

To analyze the diode leakage currents, the reverse characteristics of eutectic diodes were obtained at high voltages. Results were compared with simple $CoSi_2$ surface film diodes on comparably doped commercial Si wafers. Figure 9 compares the I-V curve traces of a eutectic diode with a carrier concentration of 3×10^{15} cm^{-3} (determined using the EBIC technique) with a Si diode having a carrier concentration of 1×10^{15} cm^{-3}.

Most notable is the difference in the behavior of the diodes at high voltage. The Si diode fails by avalanche breakdown at 125 V, while the eutectic diode remains resistive to 200 V. For the Si diode a planar junction would have led to failure at 250 V. In practice the breakdown voltage is lowered by junction curvature effects as expected for an unguarded device. The eutectic diode having a higher carrier concentration should have experienced breakdown at or below 140 V, the planar junction value. The absence of avalanche breakdown appears to be an important feature of eutectic devices and will be discussed again in Sections 5.0 and 6.0.

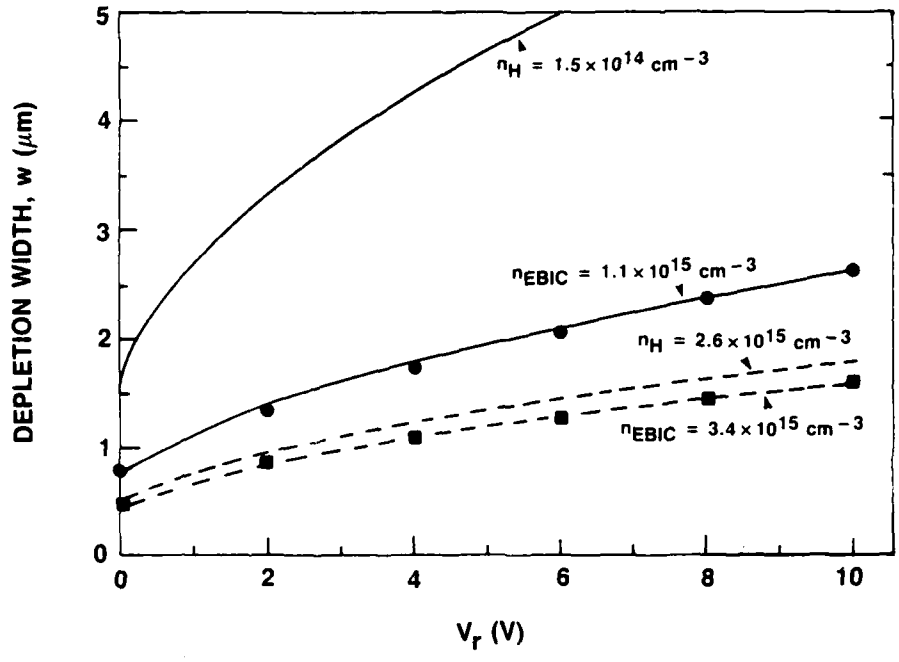
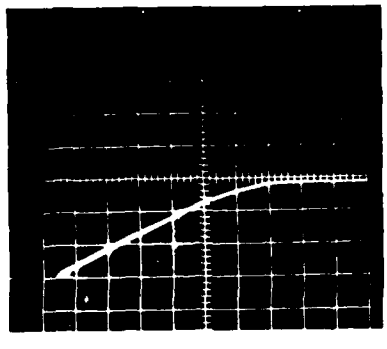
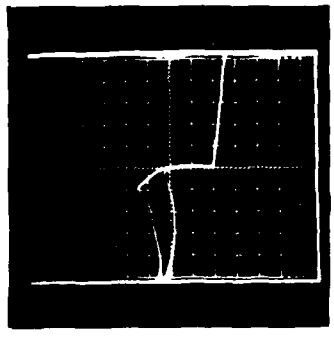


Figure 8. Depletion widths as a function of the reverse bias voltage. Two sets of solid and dashed lines correspond to two samples with different carrier concentrations. Curves are calculated using the cylindrical coordinates solution to Poisson's equation and the experimental points were derived from EBIC. n_H indicates the carrier concentration derived from the Hall effect measurements, while n_{EBIC} corresponds to the carrier concentrations derived by fitting the EBIC experimental points to the calculated curves.



5 mA/div
20 V/div

(a) Reverse bias characteristics of a eutectic diode



20 mA/div
50 V/div

(b) Forward and reverse characteristics of a planar junction Si/$CoSi_2$ Schottky diode

Figure 9. The current-voltage curve traces of (a) a eutectic diode and (b) a $CoSi_2$ planar Schottky junction diode. The area of the planar junction diode is the same as the area of the surface gate film used on the eutectic diode.

The relative leakage currents can readily be apprised in Figure 10. The $Si/CoSi_2$ junction, despite its simplicity, exhibits more leakage than can be accounted for by an analysis including Eqs. 5 and 7. Although the eutectic device contains the same $Si/CoSi_2$ junction in addition to the *in situ* junctions, it yields less reverse diode current density. At bias voltages up to about 10 V, the eutectic diode reverse current increases in a manner consistent with Eqs. 5 and 7. Beyond this bias voltage, leakage currents increase substantially. The resistance of the device in this voltage range (slope of the I-V curve) tends to saturate at a value approximately one to two orders of magnitude more than the forward bias series resistance of the device.

The above results indicate that relative to junctions produced by a simple silicidation treatment, eutectic diodes tend to be less leaky and are more resistant to avalanche breakdown. The reason for the high leakage current of the $Si/CoSi_2$ diodes is not clear, but based on experience with the Al and CVD W diodes (discussed in Section 3.2), contamination or surface layer damage may be partly responsible. It is possible that much of the leakage observed in the eutectic devices is not from the *in situ* junctions but from the leaky surface silicide film. It should also be mentioned that leakage currents can also be high on the bottom surface of the eutectic wafer since the $Si/TaSi_2$ junctions do intersect these surfaces. Attempts to distinguish between leakage at the different sites were not successful, but the possibility of the higher leakage currents being attributable to the two surfaces rather than the embedded junctions should be recognized. Improvements in surface cleanliness and polishing could lead to more ideal reverse current densities at high voltage.

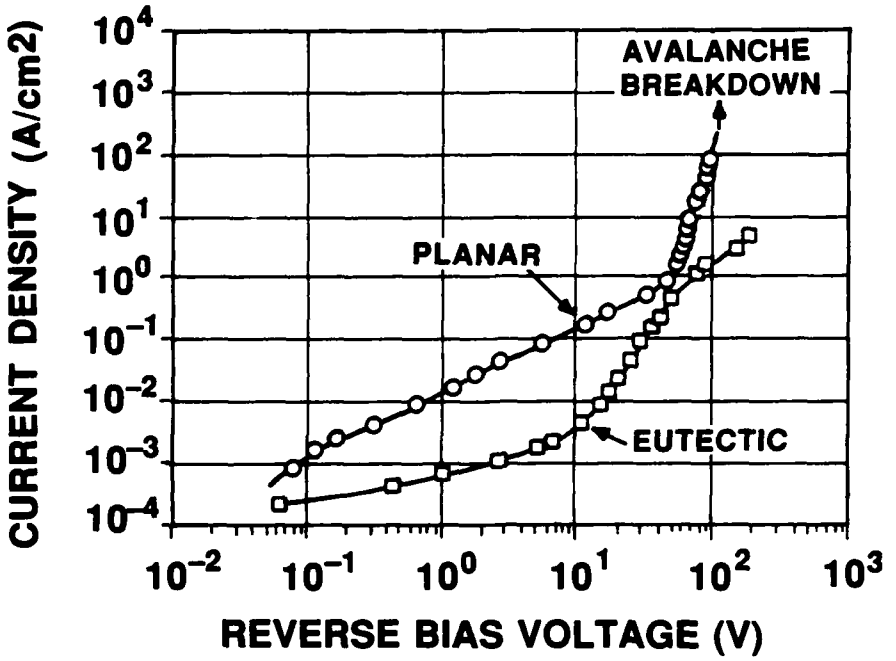


Figure 10. A comparison of the reverse bias current density (A/cm^2 of junction area) of a eutectic diode and a planar $CoSi_2$ Schottky junction diode operated at high reverse bias voltages. The planar diode avalanches at 125 V, while the eutectic diode remains resistive to 200 V, the highest voltage tested. The Si matrix carrier concentration of the eutectic diode is 3×10^{15} cm^{-3}, and the Si concentration under the planar diode is 1×10^{15} cm^{-3}.

4. EUTECTIC COMPOSITE TRANSPORT PROPERTIES

4.1 ANALYSIS OF TRANSPORT

At the beginning of this program it was clear that the transport of electrons in this composite material would be affected by the presence of *in situ* depletion zones. If depletion zones are small and do not consume a volume fraction significantly larger than the volume fraction of the second phase, $TaSi_2$, about 2%, then the composite resistivity should be that of the Si matrix. In the other extreme, if depletion zones are sufficiently large to cause intersection of depletion zones around neighboring rods, then the material should be in the "pinched-off" state and have a resistivity that is much higher than the Si matrix resistivity given by its carrier concentration and mobility.

Nevertheless, a technique for quantifying the effect of the depletion zones on resistivity was not clear. To account for this phenomena at intermediate ranges of the depletion zone volume fraction it was necessary to develop a technique for measuring the resistivity or carrier concentration of the Si matrix. The Hall effect, it was realized from previous work, did not yield a measure of the Si matrix carrier concentration as it was affected by the depletion zone volume.

As discussed in Section 3.3, EBIC provided the necessary technique for measuring the carrier concentration of the Si matrix. For a given rod diameter, since the depletion zone size is a function of the carrier concentration and the applied bias voltage only, fitting the EBIC measured depletion zone size to its functional dependence on reverse bias voltage provides a sensitive measure of the local carrier concenuration of the Si matrix.

With the Si matrix carrier concentration and the Hall effect carrier concentration, the effect of depletion zone volume on the composite transport properties was analyzed based on a model by Read.[3] Read analyzed the resistivity and Hall effect of a semiconductor with an array of parallel space-charge cylinders in a semiconductor. The model, developed long before directionally solidified eutectics were of interest, was originally applied to dislocation arrays. Read considered that the space-charge cylinders could affect transport by scattering directly from space charge cylinders, reduction in the average concentration of charge carriers, and distortion of the current streamlines.

Considering the large interrod spacings relative to the room-temperature electron mean-free path, the first effect is negligible. Hence, the actual mobility of the electrons in the semiconductor matrix will not be affected by the *in situ* depletion zones. The second effect is simple to consider; due to the volume of material in the depletion zones the carrier concentration averaged over the entire composite

volume will be less than the localized carrier concentration of material between the depleted zones. In a composite with rods of radius r_o and a rod density N_r,

$$\varepsilon = \pi(r_o + W)^2 N_r. \tag{8}$$

The average carrier concentration is given by

$$\langle n \rangle = n(1-\varepsilon). \tag{9}$$

The final effect of current streamlining was included through a definition of the current streamlining function, $g(\varepsilon)$, according to

$$g(\varepsilon) = \langle E_x \rangle_n / \langle E_x \rangle, \tag{10}$$

where the x direction is the direction of current flow, $\langle E_x \rangle_n$ is the electric field in the x direction averaged over the normal n-type material between the space-charge cylinders, and $\langle E_x \rangle$ is the applied electric field in the x direction averaged over the entire composite volume. In the limit of a very small volume fraction of depleted material (ε), $g(\varepsilon) = 1$. In the other extreme when ε approaches unity and neighboring depletion zones overlap, the voltage drop occurs primarily over the depleted volume, so that $\langle E_x \rangle_n$ and, therefore, $g(\varepsilon)$ tend to zero. An understanding of depletion zone limited transport in the eutectic composites depends on determining the $g(\varepsilon)$ function particular to the composite system.

Continuing with the Read analysis, the current density averaged over the entire composite volume, $\langle J_x \rangle$, is given by

$$\langle J_x \rangle = q\mu \langle n \rangle \ \langle E_x \rangle_n. \tag{11}$$

Substituting the measurable quantity $\langle E_x \rangle$ and the matrix carrier concentration n,

$$\langle J_x \rangle = q\mu n(1-\varepsilon)g(\varepsilon) \langle E_x \rangle. \tag{12}$$

From Eq. 12 the composite resistivity, ρ_c, is

$$\rho_c^{-1} = q\mu n(1-\varepsilon)g(\varepsilon). \tag{13}$$

Thus the ratio of the composite resistivity to the inherent resistivity of the semiconductor matrix is

$$\rho_c/\rho = [(1-\varepsilon)g(\varepsilon)]^{-1}. \quad (14)$$

Eq. 14 describes the increase in resistivity resulting from the depletion of carriers and current streamlining around the depleted zones. The composite resistivity, ρ_c, is a measurable parameter. The Hall effect measurement performed on the composite sample with the magnetic field aligned along the axis of the silicide rods provides a carrier concentration and mobility to be denoted by n_H and μ_H, respectively. Read, using an approach similar to that in Eqs. 11 and 12, showed that these parameters are related to the Si matrix carrier concentration values according to

$$n = n_H [(1-\varepsilon)g(\varepsilon)]^{-1} \quad (15)$$

and

$$\mu = \mu_H. \quad (16)$$

The Hall mobility, which depends on the ratio of electric fields and therefore cancels out the $g(\varepsilon)$ term, is independent of the current streamlining factor or the depletion zone volume fraction and represents the physical mobility of electrons in the semiconducting matrix. However, the carrier concentration derived from the Hall effect actually underestimates the semiconductor-matrix carrier concentration by the factor $(1-\varepsilon)g(\varepsilon)$. Thus, experimentally obtaining n using the EBIC technique and performing the Hall effect to obtain n_H yields the ratio of the composite resistivity to the matrix resistivity. This ratio describes the increase in composite resistivity due to depletion zone limited transport and can be related to both ε (which can also be estimated from the EBIC measurement) and $g(\varepsilon)$.

4.2 DEPLETION ZONE LIMITED TRANSPORT IN Si-$TaSi_2$ EUTECTIC COMPOSITES

Hall and EBIC measurements made on composite wafers having a rod density in the range 1.4 – 1.6 x 10^6 cm^{-3} and covering a wide Hall carrier concentration range are shown in Table 1. The ratio of the composite resistivity to the matrix resistivity is plotted in Figure 11 as a function of the actual carrier concentration, labeled by n_{EBIC} to denote the method used to obtain it. The data show that with a carrier concentration exceeding about 2 x 10^{15} cm^{-3} and ε less than about 0.05, the depletion zones have a minimal effect on resistivity. Below this critical valuc, however, ε becomes sufficiently large to cause the composite resistivity to significantly exceed the semiconductor matrix value. Since the maximum value obtained for ε is only 0.1, the analysis suggests that it is $g(\varepsilon)$, or the current

streamlining effect, that is primarily responsible for the resistivity increase. When $\varepsilon = 0.1$, $g(\varepsilon) = 0.15$. This sensitivity of $g(\varepsilon)$ to ε is suprising. Read showed that for a regular hexagonal array, $g(\varepsilon) \cong 1 - \varepsilon$ when ε is small. Thus for Read's regular lattice of space charge cylinders, $g(\varepsilon)$ would be about 0.9 and the increase in resistivity would have been minimal. The sensitivity of the eutectic composite to ε is probably attributable to the lack of regularity in the spacing of the rods and their distribution into a cellular network.

The data in Table 1 and Figure 11 are particular to eutectics with the interrod spacing shown. As a small increase in N_r can cause a significant increase in ε for a given carrier concentration, the elbow in the depletion zone limited transport curve is very sensitive to N_r. Data obtained for samples with $N_r = 2.1 \times 10^6$ cm^{-2} indicate that the elbow is closer to a carrier concentration of 3×10^{15} cm^{-3}. Similarly, a lower rod density should move the elbow to lower carrier concentrations.

Table 1. Depletion Zone Limited Transport

Sample*†	ρ_c (Ω-cm)	μ_H (cm2/Vsec)	n_H (x 10^{15} cm^{-3})	n_{EBIC} (x 10^{15} cm^{-3})	$\frac{n_{EBIC}}{n_H}\left(\frac{\rho_c}{\rho}\right)$	ε	g(ε)
1	1.0	800	7.50	8.50	1.1	0.040	0.95
2	2.9	820	2.60	3.40	1.3	0.045	0.81
3	3.0	830	2.50	3.60	1.4	0.045	0.73
4	4.4	940	1.50	2.20	1.5	0.060	0.71
5	9.0	900	0.77	1.50	1.9	0.085	0.58
6	15.7	950	0.42	1.25	3.0	0.090	0.37
7	44.6	935	0.15	1.10	7.3	0.100	0.15

*Wafers from 3 different boules

† $N_r = 1.4 - 1.6 \times 10^6$ rods/cm^2

An interesting question concerns the maximum value of the eutectic composite resistivity. Due to the segregation of P during growth, the beginning of the boules have the lowest carrier concentration and therefore the highest resistivity. With carrier concentrations just less than 10^{15} cm^{-3}, Hall carrier concentrations in the 10^{13} cm^{-3} range and resistivities as high as 600 Ω-cm have been obtained in the seed portion of boules. Thus in this region of the boule, depletion zone limited transport caused almost a factor of 100 increase in resistivity. It is likely that with additional purification or a higher growth rate, very high resistivities can be obtained.

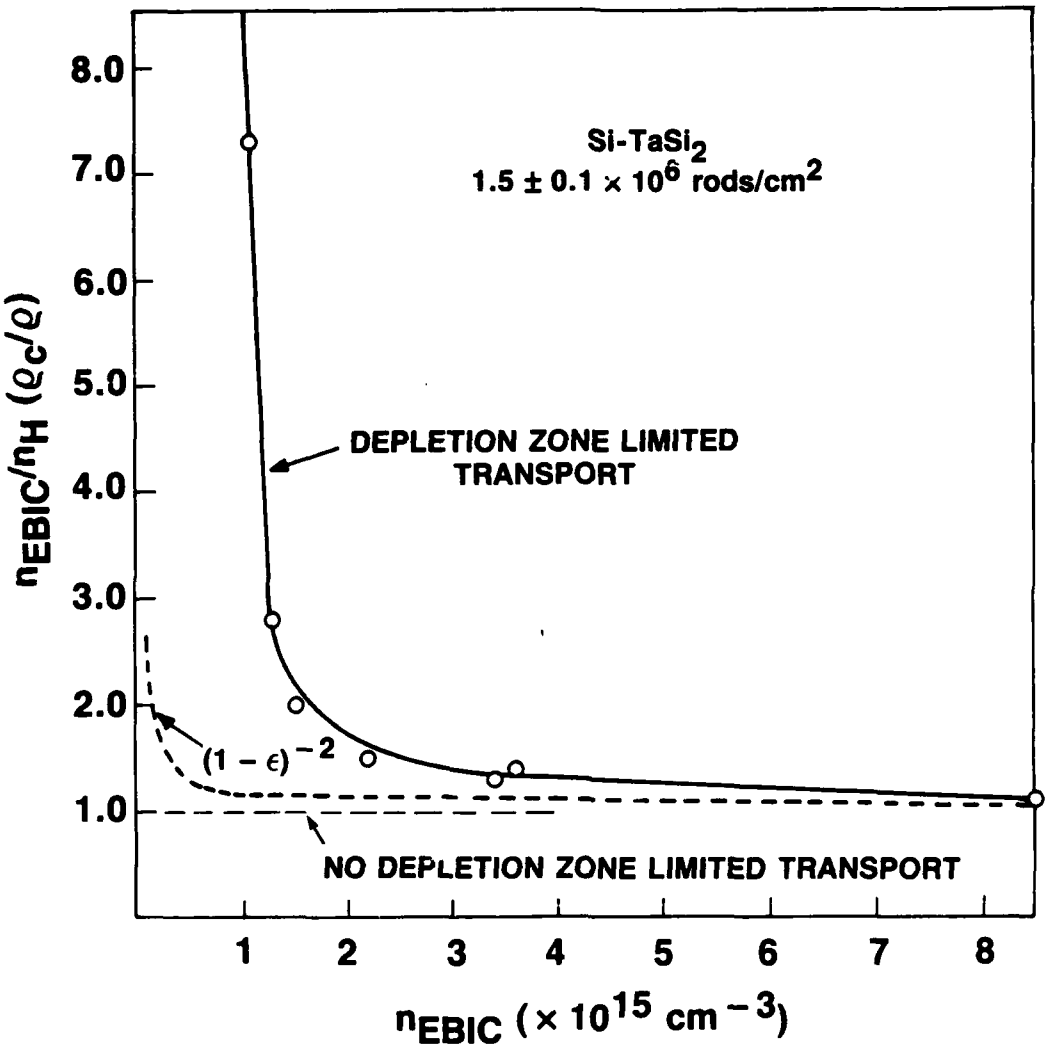


Figure 11. Correlation of the EBIC and Hall carrier concentration ratio (n_{EBIC}/n_H) [equivalently the ratio of composite to matrix resistivity (ρ_c/ρ)] as a function of the matrix carrier concentration, n_{EBIC}.

4.3 TRANSPORT AT ELEVATED TEMPERATURES

Hall effect measurements were also made at elevated temperatures as a possible means of detecting deep levels. The results proved to be rather suprising and have not been adequately explained. Measurements were made using bridge samples in a high-temperature jig that allowed testing between room temperature and 400°C. A Wacker float zone, high-purity Si crystal was used to test and calibrate the system. The Hall effect technique enables determination of the Hall coefficient, which is generally equal to[4]

$$R_H = A(nc^2 - p)/(nc + p)^2, \qquad (17)$$

where n and p are the electron and hole carrier concentrations, c is the ratio of the electron to hole mobility, approximately equal to 3 for Si, and A is a constant = $-3\pi/8q$. The expression reduces to A/n or A/p for extrinsic semiconductors doped n-type or p-type, respectively. In the event of mixed conduction, such as at elevated temperature where the semiconductor is intrinsic, Eq. (17) must be used.

The dependence of R_H on T is shown in Figure 12 for the conventional Si crystal as well as for several eutectic composite samples. This figure shows that an n-type Si-$TaSi_2$ eutectic composite grown at 2 cm/h and having only 2 x 10^5 rods/cm^2 behaves like doped Si. Below about 175°C, R_H is constant and controlled by the extrinsic phosporus dopant. Above this temperature, R_H for the composite overlaps the values for pure Si, indicating that in this temperature range the carrier concentrations are governed by activation over the Si band gap. For the composites grown at the usual rate of 20 cm/h and having the usual rod density of 2 x 10^6 rods/cm^2, R_H behaves differently. At elevated temperatures, for this case, R_H does not follow the line for intrinisic Si but tends to be smaller by nearly an order of magnitude. This trend was observed in all samples tested that were grown at 20 cm/h. Even p-type Si matrix composites converted to n-type at about 150°C and then followed the same low values for R_H as the extrinsic n-type composite samples.

Several causes for this effect were investigated. First, the possibility that strain in the Si matrix caused by the pressure of the rods resulted in a change in the composite's Si band gap was considered. Infrared transmission measurements showed unequivocally that the IR absorption cut-off and therefore the band gap were the same as for unstrained Si. A second possibility is that the low R_H values for the composite grown at the fast rate were due not to a higher carrier concentration but to a value for "c" in Eq. 17 that tended toward 1. A large drop in the electron mobility at elevated temperature relative to the hole mobility would be required. Such a situation is considered to be

unlikely since at room temperature the c-value of 3 has been observed and the mean free path decreases, rather than increases, with temperature, suggesting that the high rod density should not limit the mean free path at elevated temperature if it doesn't at room temperature. A third potential cause is the presence of interface states and deep levels. As the rod density increases, the interfacial area increases and so should interface states. For the high rod density case, each cubic centimeter of material contains approximately 500 cm^2 of silicide/Si interface. With an interface state density of about 10^{15} cm^{-2}, a significant number of carriers may be generated at elevated temperature. The effect of deep levels was examined by solving the charge neutrality equation for various different deep levels and concentrations. Though this can alter the carrier concentrations at elevated temperatures, the concentrations required were considered too high to be realistic. Thus, though several possible explanations for this effect have been presented, none satisfactorily explains it.

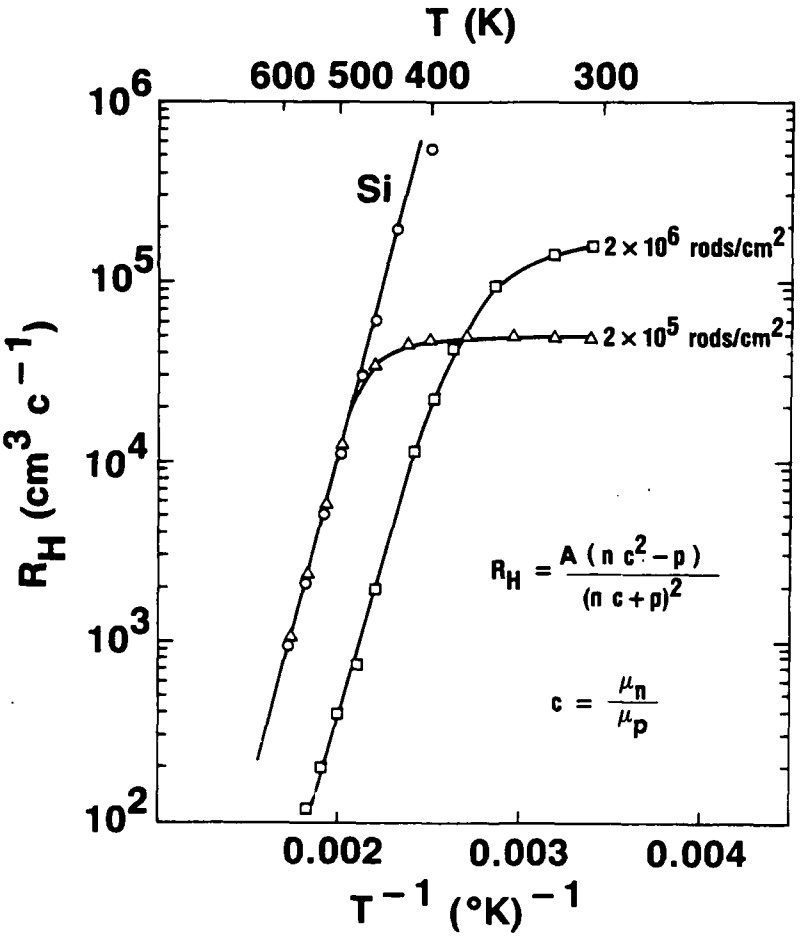


Figure 12. The Hall coefficient of the eutectic composites at elevated temperature depends on the growth rate or interrod density.

Device operation must be limited to temperatures below which R_H is nearly constant. Thus the decrease in R_H may act to limit the maximum temperature of operation below that for a conventional Si device. For eutectic devices with a typical carrier concentration of about 1×10^{15} cm^{-3}, operation would probably have to be limited to about 125°C. During testing of devices at high-power levels (about 10 W), thermal runaway has been observed, but similar observations are made for conventional Si FETs. The volumetric distribution of the junctions may offset the adverse effects of the high-temperature carrier concentrations suggested by Figure 12.

5. TRANSISTOR ACTION IN Si-$TaSi_2$ EUTECTIC COMPOSITES

5.1 TRANSISTOR DESIGN AND FABRICATION

To demonstrate "pinch-off" in a eutectic transistor, a simple concentric circle design for the source, drain, and gate contacts was used. A quarter section of the surface contacts of a typical device is shown in Figure 13(a). In this device, the outside ring acted as the source and the inside dot as the drain contact. Current moving from the source to the drain must pass under the centrally located gate. Thus, biasing the gate should enable device "pinch-off." This simple design was used as a vehicle for testing the characteristics of the device and its dependence on material and device design parameters. Higher current, pulsed power devices would require a more sophisticated design.

Formation of the device contacts proceeded similarly to those already discussed for diode contacts. In the first fabrication step, the wafers were thermally oxidized at 1000°C to grow a 0.3-μm-thick oxide. Vias in the oxide were opened lithographically for the surface contacts. The gate contact was formed by the direct silicidation of an evaporated Co film at 800°C to form a surface film of $CoSi_2$. Figure 13(b) shows a SEM micrograph of the $CoSi_2$ gate contact film with the $TaSi_2$ rods beneath it. Different device designs were employed, including one in which the gate contact ring had an enlarged dot to enable good contact with a probe. The source and drain contacts were fabricated using annealed, evaporated Au-Sb films. In certain cases, $CoSi_2$/ n^+ contacts were used for the source and drain.

Dimensional parameters affecting device performance are the gate contact width, the source-to-gate and gate-to-drain spacings, and the wafer thickness, which also corresponds to the gate length. Several different mask sets were employed to evaluate the effect of these parameters. Gate width was varied between 20 μm and 125 μm. The gate- to-drain and gate-to-source spacings ranged from 62 μm to 180 μm. Devices were tested in wafers varying in thickness from 125 μm to 500 μm.

5.2 BASIC TRANSISTOR CHARACTERISTICS

An example of the current-voltage characteristics of a eutectic composite transistor with the drain current plotted against the drain voltage for different gate voltages is shown in Figure 14. The basic characteristics of the device are similar to those of a conventional metal-semiconductor field-effect transistor (MESFET) in that they display a linear region and a saturation region. Several points may be made regarding the basic characteristics of the eutectic device.

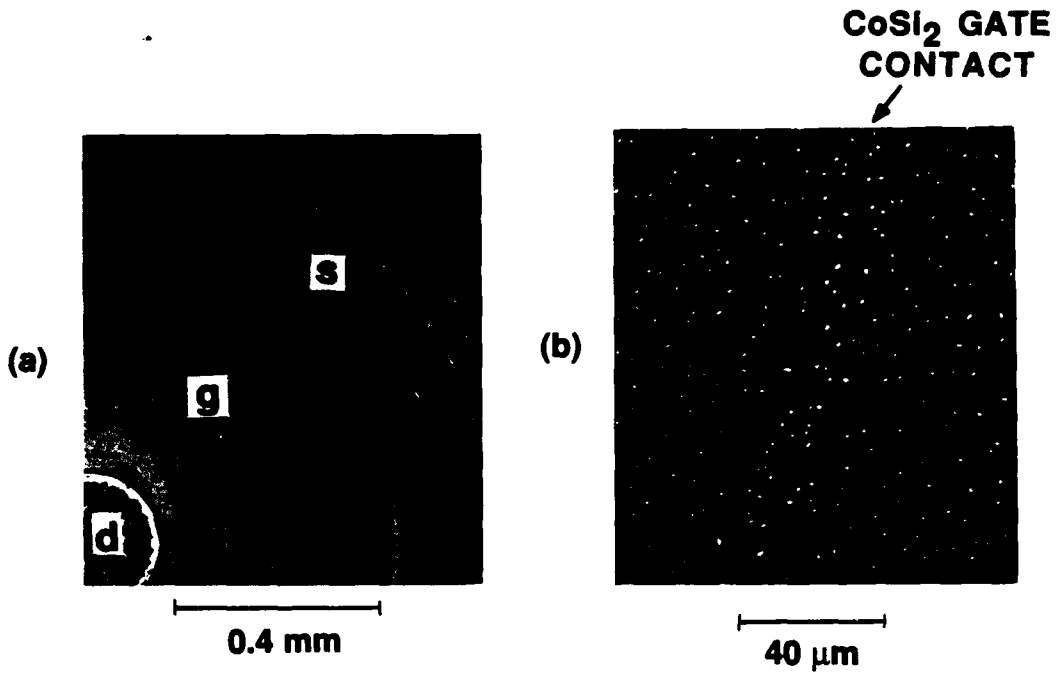


Figure 13. Quarter section of a Si-$TaSi_2$ eutectic composite transistor is shown in part (a). In this device the source *s* and drain *d* contacts are made with a Au-Sb contact and the gate *g* contact is a $CoSi_2$ film. Part (b), a closeup of the gate ring, shows the size and distribution of the $TaSi_2$ rods.

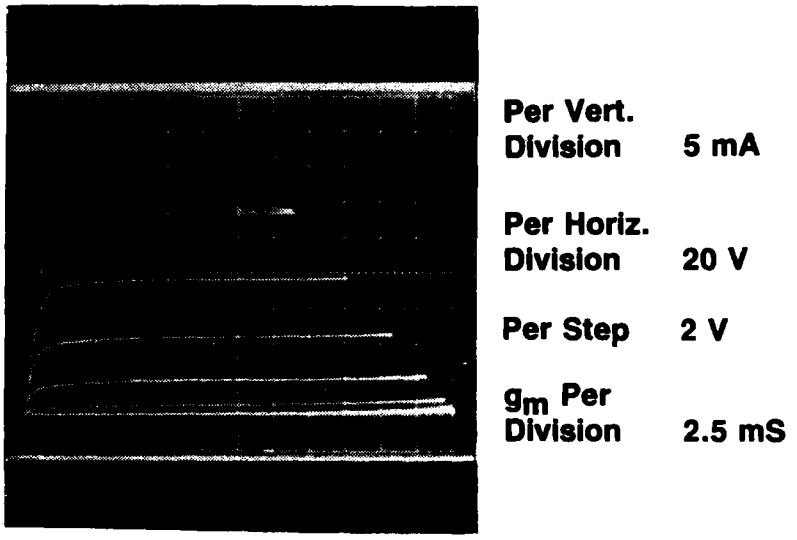


Figure 14. Characteristics of a Si-$TaSi_2$ eutectic composite transistor. A 10 V reverse bias is required to "pinch off" the device.

1. The series resistance of the device, taken as the slope of the unbiased curve in the limit of small drain voltages, is 400 Ω. In light of the composite resistivity and the device dimensions, this value indicates that the entire thickness of the device is being used for the current channel.
2. The "pinch-off" condition for this device corresponds to –10 V. This particular wafer had an average interrod spacing of 6.9 μm. Thus for the average 1-μm-diameter rod, an average of 4.9 μm of Si matrix separates two rods spaced exactly by the average interrod spacing. With the –10 V pinch-off voltage, the depletion zone around each rod should extend 2.0 μm from each rod/matrix interface. Thus a –10 V bias, leaving 0.9 μm of undepleted Si between channels, should not enable pinch-off. This simple analysis suggests that the pinch-off condition may not be determined solely by the average interrod spacing but by the spacing of the nearest neighbor rods. A similar conclusion was made concerning the effects of depletion zone limited transport.
3. The degree of pinch-off of the device depends sensitively on the carrier concentration. Good devices can be fabricated only in wafers that have carrier concentrations corresponding to the elbow or the low carrier concentration leg of the depletion zone limited transport curve in Figure 11. For this rod density, wafers with carrier concentrations exceeding about 4×10^{15} cm^{-3} were always too leaky to exhibit any significant "pinch-off." It is similarly true that low leakage diodes could not be fabricated in this carrier concentration/rod density range. The few data obtained on higher rod density samples do suggest that higher rod densities enable the fabrication of devices with higher carrier concentrations.
4. The drain current in the pinch-off condition, defined as that point at which an increase in the bias voltage does not result in a decrease in the drain current, was found to vary significantly from device to device. Measured at a drain voltage of 200 V, minimum drain currents in the pinch-off condition were about 2% of the unbiased saturation drain current. Thus in a device with a 20 mA saturation current, minimum drain current with a –12 V bias at a drain voltage of 200 V was 400 μA. This may be high compared to Si p-n junction devices, but it was considered to be quite low for these 0.62 eV Schottky barrier devices. In general, transistor leakage currents were significantly lower than diode reverse bias currents when compared for similar surface contact areas.
5. In conventional devices the drain voltages are limited by avalanche breakdown. The carrier concentration of the wafer on which the device in Figure 14 was fabricated was 2×10^{15} cm^{-3}. For a conventional planar device, a similar n-type carrier concentration would break down by an avalanche effect at 190 V. The eutectic device, however, is blocking 240 V, as shown. The device actually failed at 325 V, significantly exceeding the planar junction value. Failure was not by avalanche breakdown but by a catastrophic mechanism that destroyed the device characteristics.

The reason for the eutectic device's resistance to avalanche breakdown and the mechanism of failure are very interesting and are examined in detail. The following section is devoted to experiments to probe the high voltage features of the device.

5.3 HIGH VOLTAGE EFFECTS

The effects of several changes in device design parameters on the device breakdown voltage are shown in Table 2. For four different devices the table gives the carrier concentration and resistivity of the wafer, the gate-to-drain (g-d) distance, the wafer thickness, and the voltage at breakdown, Vmax. An important observation was the effect of wafer thickness on the failure voltage. The device labeled SiTa 61 #25 is a good example; the characteristics of the device are shown in Figure 15(a) and (b) for thicknesses of 250 μm and 125 μm, respectively. Initially this device was tested at a 500 μm thickness and failed prematurely, before a photograph could be taken, at 45 V. After thinning the wafer from the side opposite that with the surface contacts, the same device was retested. Thinning the wafer resulted in the recovery of the device and yielded the characteristics in Figure 15(a). Though leaky at the high drain voltages, the device is shown blocking a drain voltage of 300 V with a gate voltage of –10 V. The unbiased curve is cut off at low voltages because a high series resistor was used in the curve tracer to minimize heating effects. This device failed catastrophically when taken to a drain voltage of 325 V. The wafer was thinned further to 125 μm, and the device was retested. The characteristics of the same device in the thinned wafer are shown in Figure 15(b). Again the device recovered and operated with a drain voltage of 600 V. This value is at least three times the blocking voltage of a conventional planar device in a wafer of the same carrier concentration. Throughout these thinning experiments it was also found that the saturation decreased proportionately to the wafer thickness, indicating further that the entire wafer acts as the current channel. As can be seen in Table 2, the effect of thickness on breakdown voltage was consistently observed.

Table 2 also shows that breakdown voltage increases with gate-to-drain spacing. This implies that the failure mechanism is related to "punch-through" of the depletion zone extending from the gate to the drain. A model based on this failure mode can be used to explain the thickness effect. The basis for the model is schematically illustrated in Figure 16. As is clear from longitudinal micrographs of the surface and EBIC studies, the rods do not align perfectly and may diverge from the wafer normal by as much as 6°. Thus as shown in the figure, the separation of the drain and gate contacts is the smallest at the bottom surface of the wafer, and the actual minimum separation depends on the wafer thickness. In the example in the schematic, a 140 μm gate-to-drain distance may be reduced to as little as 40 μm on the backsurface of a 500-μm-thick wafer due to a 6° rod divergence.

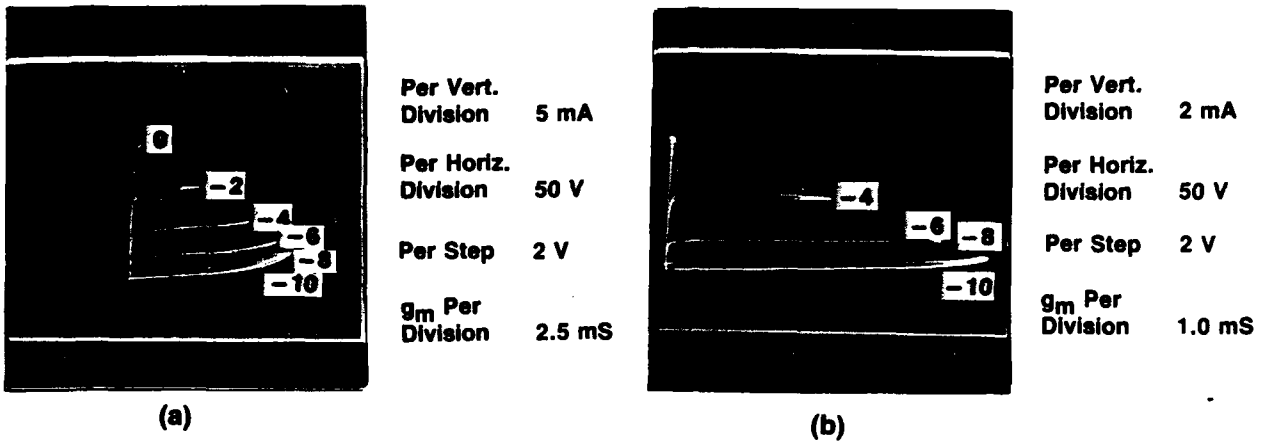


Figure 15. Characteristics of a Si-$TaSi_2$ eutectic composite device tested with a wafer thickness of 250 μm (a) and after thinning to a wafer thickness of 125 μm.

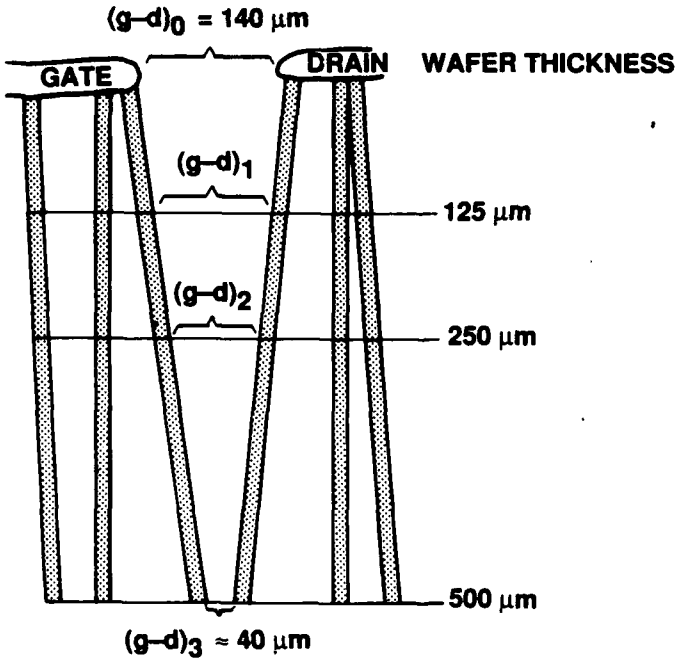


Figure 16. A schematic showing how the divergence of the rods can reduce the gate-to-drain distance on the back surface of the wafer relative to the dimensions lithographically positioned on the top surface.

Table 2. Factors Affecting the Maximum Blocking Voltage

Wafer	Carrier Concentration (10^{15})	Resistivity (Ω-cm)	g-d Distance (μm)	Thickness (μm)	Vmax (V)
SiTa 61 #25	3	8	137	500	50
SiTa 61 #25	3	8	137	250	350
SiTa 61 #25	3	8	137	125	600
SiTa 61 #41	2	12	150	500	90
SiTa 61 #41	2	12	150	250	250
SiTa 61 #41	2	12	150	125	500
SiTa 59 #31	1	18.5	180	250	500
SiTa 59 #31	1	18.5	180	125	700
SiTa 59 #47	1	50	62	250	40

The results for the breakdown voltage appear consistent with a "punch-through" model. If punch-through is occurring at V_{max}, then the size of the depletion zone at failure may be approximately determined. Consider the case for the 125 μm device on SiTa 61 #25. The gate-to-drain spacing on the bottom of the wafer must be about 115 μm at V_{max} = 600 V. Thus, at failure, the depletion zone size must be approximately 115 μm. This indicates a considerably higher value than the 40 μm expected for a conventional Si planar junction that fails by avalanche breakdown at 600 V. For the eutectic device the average field in the depletion zone is about 50 kV/cm, one third the value of the planar case.

The implication of a reduced field and a longer depletion zone size for the eutectic device may also explain the device's resistance to avalanche breakdown (as well as its low leakage currents). For a comparable carrier concentration, the depletion zone may extend further for a eutectic device than a conventional device. An explanation for this effect is presumed to be related to the interaction of the depletion zone around the gate rods with the floating rods between the gate and the drain. This effect was modeled as part of a program funded by SDIO/IST and managed by ONR and is reported in the following section for completeness.

6. RECENT ADVANCES

6.1 DEVICE MODELING

Recently, additional research on semiconductor-metal eutectic devices has been initiated as a result of SDIO/IST and GTE funding that bears directly on the anlaysis of the feasibility of using eutectic composite devices in pulsed power operation. The first concerns the analysis of the device's resistance to avalanche breakdown and the second, the RF characteristics of the device. These studies, both in a preliminary stage, are reported here.

PISCES, a finite differences computer simulation model, has been used to model the characteristics of the eutectic composite transistors. This code permits the modeling of two-dimensional distributions of potential and carrier concentrations of arbitrary device geometries for any bias conditions. The code limits the number of electrodes to 9; thus with two electrodes for the source and drain contacts, the model enables inclusion of at most 7 rods. Because of this limitation, it is difficult to model a geometry that reflects the true distribution of the $TaSi_2$ rods. Nevertheless, it is useful for the demonstration of concepts, such as the effect of floating rods on the depletion zone size around the gate. To evaluate this factor the four different geometries shown in Figure 17(a) were simulated. In each configuration the rod closest to the source acted as the gate, and the remaining 6 rods were left floating. Geometry 1 simulates the conventional device without any floating rods, while geometries 2, 3, and 4 have the floating rods with separations of 5 μm, 7 μm, and 10 μm, respectively. Due to the limitations on the number of rods, the spacing between the floating rod closest to the drain and the drain differs in each case. Since the eutectic devices have rods extending to the drain, this feature of the geometry modeled is unrepresentative and results in the region should be ignored.

Graphs of the (1) potential between source and drain for a 200 V drain voltage and a –2 V bias and the (2) maximum electric field (occurring at the gate rod on the side of the drain) with a –2 V bias between 0 and 200 V drain voltage is shown in Figure 17(b) and 17 (c), respectively. From these figures it is clear that in the conventional case, line #1, the potential drops off parabolically, and the maximum electric field continues to increase as the drain voltage is increased. In cases #2-#4, the interaction of the depletion zone at the gate rod with the floating junctions clearly affects the potential drop, the maximum electric field, and the extent of the depletion zone. For the eutectic-like microstructures, the potential drop decreases parabolically between rods such that the potential drop between each rod is approximately constant. Thus, the field reaches a maximum when the drain voltage is sufficient to extend the depletion zone to the first floating rod and then remains at the

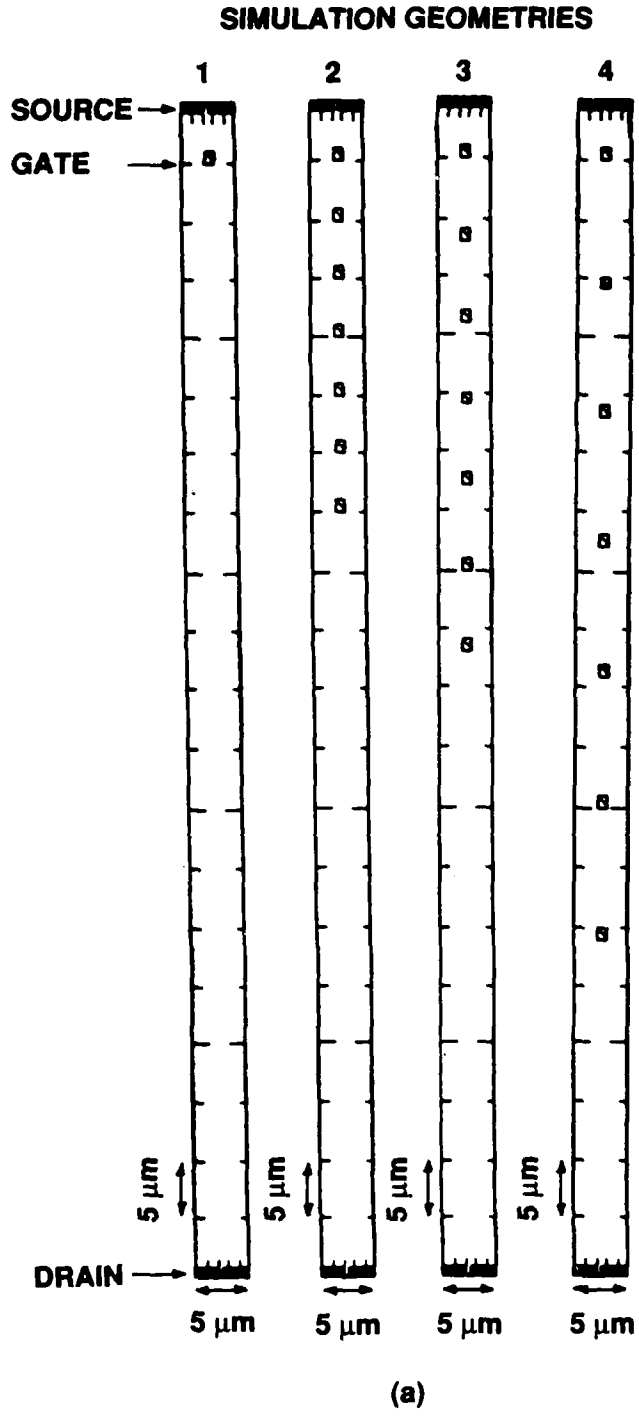
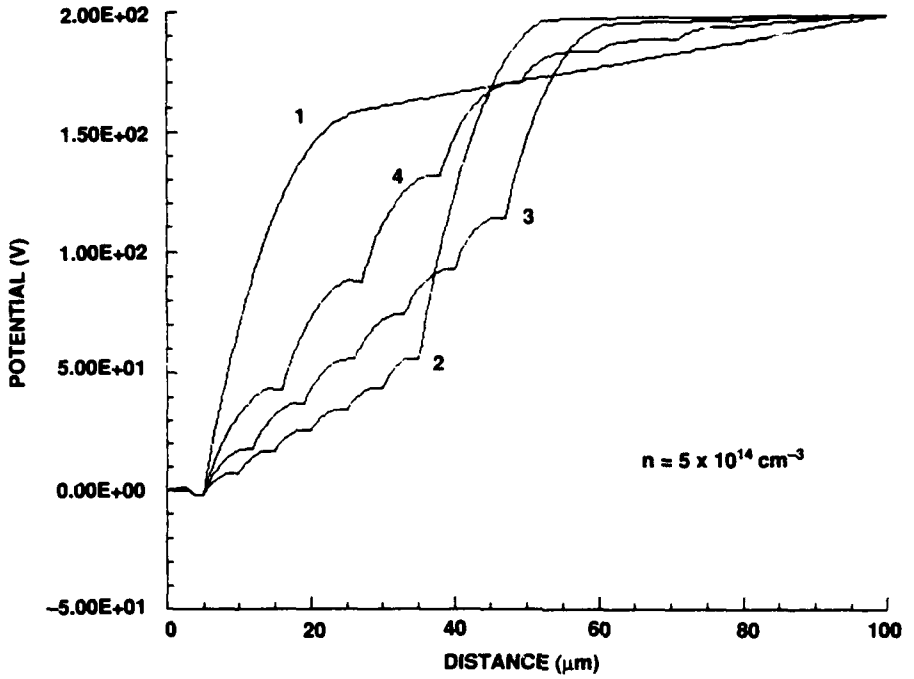
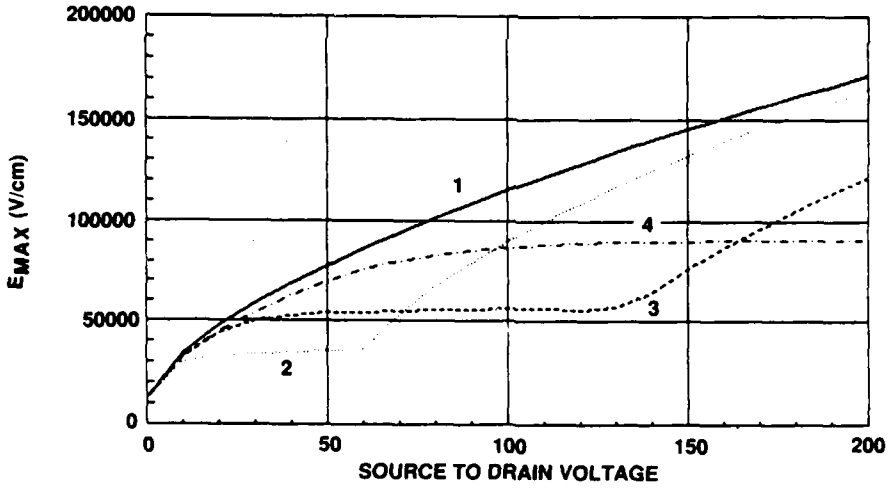


Figure 17. PISCES model of the effect of floating rods on the depletion zone extending from the gate and the potential and field distributions between the gate and drain on simulated eutectic geometries: (a) shows the four geometries modeled. In each case the rod closest to the source acts as the gate and the remaining rods are left floating. (b) displays the potential between source and drain for a 200 V drain voltage and a –2 V bias for each geometry. Similarly, for each geometry, (c) shows the maximum electric field incurred with a –2 V bias as the drain voltage is increased from 0 to 200 V.



(b)



(c)

Figure 17. Continued.

maximum as the drain voltage is increased. The maximum field achieved is much lower than the field for the classic case without floating junctions, with the actual value depending on the spacing of the junctions.

This result clearly establishes that the floating rods in the eutectic transistor devices inhibit avalanche breakdown and result in larger depeletion zones than would be expected for a classical planar junction device. In a conventional device without floating rods, the maximum electric field increases as the drain voltage increases until it reaches the critical value for avalanche breakdown. With the floating rods, however, the field reaches a maximum as the drain voltage is increased that is significantly lower than the critical field for avalanche breakdown. Thus, even as the drain voltage is increased to a value significantly beyond that required to yield avalanche breakdown in a conventional device, avalanche breakdown is avoided because the field never reaches a value sufficient to cause impact ionization. However, since the depletion zone extends further than the expected depletion zone for a conventional device without floating rods, the device may fail by a "punch-through" mechanism if the gate-to-drain spacing of the device is not designed to accommodate this effect.

The model's predictions are in good agreement with the experimental results. As discussed in the previous section, analysis of the maximum drain voltage at device failure indicates that the depletion zone extends significantly beyond the classic planar junction value.

The model is important for the understanding and development of eutectic devices for several reasons. First, it indicates that an ideally designed device may block a very high voltage unlimited only by the device's size. Since it has already been demonstrated that average fields of 50 kV/cm can be supported, the model suggests than a gate-to-drain spacing of 1 cm can result in a device that will block 50 kV, a value more than an order of magnitude higher than can currently be blocked by conventional power devices. Second, the model may be a powerful tool for the optimization of the microstructure/carrier concentration relationships for pulsed power operation. Optimized devices would support a maximum electric field that was just below the critical value for breakdown. This would enable a higher current in a minimum gate-to-drain spacing device.

6.2 RF CHARACTERISTICS

The speed of eutectic devices is also pertinent to their evaluation for pulsed power device operation. Consequently, preliminary measurements of the RF characteristics of a eutectic composite device are discussed. Measurements were made between 300 kHz and 300 MHz on a device operated with a

drain voltage of 30 V and a –2 V bias. The preliminary measurements indicated a maximum frequency of oscillation of about 50 MHz. This value is lower than the limitation imposed by the RC time constant for this device of about 120 MHz. Analysis indicates that the device speed is limited by the device design which consisted of a gate ring 62 μm inside of the source contact. The resistance drop across this length can effectively bias the gate and reduce the device transconductance. Designing devices for high frequency and speed would require a significant reduction in the source to gate spacing.

Based on these limited studies and calculated minimum RC time constants, optimized Si-$TaSi_2$ devices may be expected to operate at high voltage at frequency limits in the range of 0.5 GHz. Advanced eutectic materials, such as GaAs-based SME materials, could raise this limit to about 2.5 GHz.

7. IMPLICATIONS FOR PULSED POWER

The implications of the results presented in this report for high-voltage pulsed power switching are intriguing. Even though experimentally the maximum voltage blocked by these first eutectic devices is only 700 V (small by pulsed power standards but large for conventional Si FETs), the model suggests that significantly higher voltages could be handled. It appears that it is only the small scale of these test devices, particularly the gate-to-drain distance (a maximum of 180 μm tested), that is limiting the maximum blocking voltage of the eutectic devices. According to the model and the experimental results, a gate- to-drain spacing of 1 cm could lead to a 50 kV blocking voltage. In practice the simple recipe which states simple device length times maximum average field yields blocking voltage may be limited by excess leakage currents. Only actual testing at high voltage levels can answer these questions. In any event, it is likely that this simple device fabrication route can lead to higher voltage transistors than can be developed using conventional device concepts.

The maximum current of these devices in the "on-state" may be more of an issue than blocking voltage. In general, very large currents can be achieved by using devices of large cross-sectional area and connecting them in parallel. But the saturation of the drain current at drain voltages of only 15 - 20 V may limit the current flowing in the load resistor. As an example using 10 Ω-cm composite material with a gate-to-drain distance of 0.1 cm may be expected to yield a device that can block about 10 kV and have a saturation current of about 20 A per cm^2 of source and drain area. This assumes the pulse is sufficiently short to avoid heating effects. If the device did not saturate, the "on-state" current through the load resistor would be limited by that resistor and not by the series resistance (~1 Ω) of the eutectic switch.

Though the SME materials clearly portend advances in high voltage switching, advanced research on this new subject continues to be needed. In general these studies would be expected to lead to devices optimized for current handling and voltage blocking capability through the development of new materials, device designs, and an improved understanding of the basic physical phenomena. Suggested areas for additional studies are briefly discussed in the following.

1. Devices must be designed with large gate-to-drain spacings and tested at high voltages. Factors affecting maximum blocking voltages must be evaluated and compared to model results. Device speed, thermal effects, and leakage currents of devices operated in this high-voltage range should be evaluated.
2. Methods for decreasing the series resistance of the device should be developed. These would be expected to include development of composites with higher interrod spacings in order to enable

use of higher carrier concentration, lower resistivity composite material. A rod density that would enable a carrier concentration of 10^{16} cm^{-3} would result in a factor of 10 increase in saturation current. Furthermore, GaAs-based composites must be developed. The higher mobility of GaAs relative to Si would lead to about a factor of 5 enhancement of saturation current in the above example for a similar microstructure and carrier concentration.

3. The mechanism for the saturation of the eutectic devices should be rigorously investigated in order to evaluate methods for fabricating devices with the triode-like characteristics of vertical junction FET devices. This may result simply from decreasing the gate width below the 20 μm minimum value examined in this study. With non-saturating characteristics, the eutectic devices are expected to surpass the current density limits, as well as the blocking voltage limits, of conventional Si devices.
4. The device physics and materials research discussed in the first three examples must be supported with research aimed at improving the understanding of the directional solidification and crystal growth of semiconductor-metal eutectics. Factors leading to the cellular distribution of rods, the misalignment of rods, and large-scale variations in rod density must be more thoroughly examined.

8. REFERENCES

1. S.M. Sze, *Physics of Semiconductor Devices* (Wiley, New York, 1969).

2. J.M. Andrews and M.P. Lepselter, IEEE Solid State Device Conf., Washington D.C. (October 1968).

3. W.T. Read, Philos. Mag. 46, 111 (1955).

4. E.H. Putley, The Hall Effect and Semiconductor Physics (Dover Publications, Inc., New York, 1960).

9. LIST OF PUBLICATIONS

1. B.M. Ditchek and M. Levinson, "Si-$TaSi_2$ *in situ* Junction Eutectic Composite Diodes," *Appl. Phys. Lett. 49*, 1656 (1986).

2. B.G. Yacobi and B.M. Ditchek, "Characterization of Multiple *in situ* Junctions by Charge Collection Microscopy," *Appl. Phys. Lett. 50*, 1083 (1987).

3. B.G. Yacobi and B.M. Ditchek, "EBIC Characterization of Multiple *in situ* Three-dimensional Junctions in Silicon," the 5th Oxford Conference Proc. on Microscopy of Semiconducting Materials, Oxford University, Oxford, England, p. 703 (1987).

4. M. Levinson, B.M. Ditchek, and B.G. Yacobi, "Capacitance Spectroscopy of Si-$TaSi_2$ Eutectic Composite Structures," *Appl. Phys. Lett. 50*, 1906 (1987).

5. B.M. Ditchek, B.G. Yacobi, and M. Levinson, "Semiconductors with Built-In Junctions," *GTE J. of Sci. and Tech. 1*, 2 (1987).

6. B.M. Ditchek, T.R. Middleton, P.G. Rossoni, and B.G. Yacobi, "Novel High Voltage Transistor Fabricated Using the *in situ* Junctions in a Si-$TaSi_2$ Eutectic Composite," *Appl. Phys. Lett. 52*, 1147 (1988).

7. B.M. Ditchek and B.G. Yacobi, "Semiconductor-Metal Eutectic Composites for High Power Switching," SPIE Vol. 871, Space Structures, Power, and Power Conditioning, p. 148 (1988).

8. B.M. Ditchek, B.G. Yacobi, and M. Levinson, "Depletion Zone Limited Transport in Si-$TaSi_2$ Eutectic Composites," *J. Appl. Phys. 63*, 1964 (1988).

9. B. M. Ditchek, T.R. Middleton, K.M. Beatty, and J.A. Kafalas, "Directional Solidification of Si- and GaAs-Based Eutectics for Electronic Applications," The Metallurgical Society Meeting Conf. on Directional Solidification of Eutectics Conf. Proc., Cincinnati, OH (October 12-16, 1987).

10. LIST OF PRESENTATIONS

1. B.M. Ditchek, "Semiconductor-Metal Eutectic Composites," at Georgia Inst. of Tech., Atlanta, GA (November 12, 1986).

2. B.G. Yacobi and B.M. Ditchek, "EBIC Characterization of Multiple *in situ* Three-dimensional Junctions in Silicon," at the 5th Oxford University Conf. on Microscopy of Semiconducting Material, Oxford, England (April 7, 1987).

3. B.M. Ditchek, T.R. Middleton, K.M. Beatty, and J.A. Kafalas, "Directional Solidification of Si- and GaAs-Based Eutectics for Electronic Applications," The Metallurgical Society Meeting on Directional Solidification of Eutectics Conf. Proc., Cincinnati, OH (October, 12-16, 1987).

4. B.M. Ditchek and B.G. Yacobi, "Semiconductor-Metal Eutectic Composites for High Power Switching," SPIE Conf. on Space Structures, Power, and Power Conditioning, part of the 1st Symposium, Los Angeles, CA (January 11-13, 1988).

11. LIST OF PATENTS SUBMITTED

1. B.M. Ditchek, E. Sichel, A. Cogan and W. Bloss III, "Semiconductor Device," submitted to U.S. Patent Office, Serial No. 941478, filed on December 11, 1986.

2. B.M. Ditchek, "Method of Producing a Semiconducting Device," Serial No. 940371, filed on December 11, 1986.

3. B.M. Ditchek, M. Levinson, and B.G. Yacobi, "Radiation Detecting Apparatus," Serial No. 020629, filed on March 2, 1987.

12. LIST OF PATENTS ISSUED

1. B.M. Ditchek, "Method of Making Electrical Contacts," U.S.Patent No. 4,724,223, issued February 9, 1988.

13. PROFESSIONAL STAFF

Dr. Brian M. Ditchek and Dr. John G. Gustafson, Principal Investigators

Dr. Ben G. Yacobi, Senior Member of the Technical Staff

Dr. M. Levinson, Principal Member of the Technical Staff

Appendix – reprints and preprints of publications submitted with the support of this contract.

Appendix A

Si-$TaSi_2$ *In Situ* Junction Eutectic Composite Diodes

Si-$TaSi_2$ *in situ* junction eutectic composite diodes

Brian M. Ditchek and Mark Levinson
GTE Laboratories, Incorporated, 40 Sylvan Road, Waltham, Massachusetts 02254

(Received 15 September 1986; accepted for publication 6 October 1986)

Nearly ideal diodes have been fabricated using the *in situ* junctions present in Si-$TaSi_2$ semiconductor-metal eutectic composites. The composites, prepared by directional solidification at the eutectic composition, have a high density of $TaSi_2$ rods in a quasi-single crystalline P-doped, *n*-type Si matrix. Analysis of the diodes using current-voltage and capacitance-voltage techniques yields a $TaSi_2$/Si Schottky barrier height of 0.62 eV and evidence that the voltage-dependent depletion zones can be made comparable to the interrod spacing to produce a "pinch-off" condition.

Directional solidification of eutectic mixtures commonly yields composite materials having a rodlike or lamellar distribution of phases.[1] In semiconductor-semiconductor or semiconductor-metal systems this can result in materials with a three-dimensional array of rectifying junctions. Besides providing a means for the microelectronic characterization of the semiconducting phase, diodes based on these junctions could in principle be the basis for high power field-effect transistors or novel large area photodiodes and photovoltaic devices. Due to their potential for such devices, many semiconductor-based eutectics have been grown and microstructurally characterized. For example, rodlike eutectics have been found in directionally solidified GaAs-VAs,[2] GaAs-Ge,[3] InSb-NiSb,[4] and several Ge-metal germanide[5–7] and Si-metal silicide[5–8] systems. Lamellar structures have been reported in CdTe-GaTe[9] and SnSe-$SnSe_2$.[10] Of these systems, initial diode characterization of the *in situ* junctions was performed in the latter two systems only. In both cases, though diode current-voltage (*I-V*) characteristics were reported, interpretation of these characteristics in terms of barrier height, junction area, or depletion zone width was not performed.

In this letter we report the fabrication and electronic characterization of high quality Si-$TaSi_2$ composite diodes with a rodlike distribution of the metal phase. Unlike the lamellar structures previously studied, the Si-$TaSi_2$ eutectic was prepared with a single crystalline Si matrix in which the donor concentration could be controlled during growth and measured using the Hall effect. In addition, since diodes were fabricated using techniques that allowed the determination of total junction area, the diode characteristics could be analyzed.

The Si-$TaSi_2$ eutectic composites were grown directly from the melt in a Czochralski crystal growth furnace in much the same way as Si single crystals. A charge of Si-5.5 wt. % Ta was placed in a quartz crucible contained in a graphite susceptor. After rf heating the charge to above the eutectic temperature, a (111) Si seed was lowered to the melt surface. Composite boules were pulled from the melt at 20 cm/h in a flowing Ar atmosphere. Carrier type and concentration were determined by the P-doped Si intentionally added to the charge. Boules grown this way were quasi-single crystals; that is, the 2 vol %, rodlike distribution of metallic $TaSi_2$ was contained in a grain boundary-free, (111) Si matrix phase. Czochralski growth has been similarly found to yield quasi-single crystal composites in the Ge-$TiGe_2$ system.[7] The scanning electron micrograph in Fig. 1 shows the microstructure of a wafer cut transverse to the growth direction followed by polishing and etching away the Si surface to expose the $TaSi_2$ rods. The composite grown at this rate contains 1.6×10^6 $TaSi_2$ rods/cm^2 with an average rod radius of 0.6 μm.

Devices were prepared from a P-doped, *n*-type boule approximately 2.5 cm in diameter and 12 cm long. Wafers were cut transverse to the growth direction along the entire length of the boule. Bridge-type Hall samples were prepared from wafers at several different positions along the boule length so that the variation in carrier concentration and electron mobility along the length of the boule could be determined. Since the carrier concentration in the boule varied only modestly from one end to the other, $N_d = 1.1\times10^{15}$ cm^{-3} to $N_d = 1.8\times10^{15}$ cm^{-3}, the carrier concentration in wafers used for diode fabrication was accurately known. Electron mobility in all wafers tested was approximately 925 cm^2/V s. (For a discussion of the Hall effect in rodlike semiconductor-metal eutectic composites see Ref. 6.)

Diodes were fabricated on 500-μm-thick wafers polished using colloidal silica. Contacts were made to the $TaSi_2$ rods by the formation of a 0.2-μm-thick surface metallic film of $CoSi_2$. In the first step a 0.2-μm-thick oxide was grown. The $CoSi_2$ film was then formed selectively in a 127-μm-wide opening in the oxide using rapid thermal annealing of a

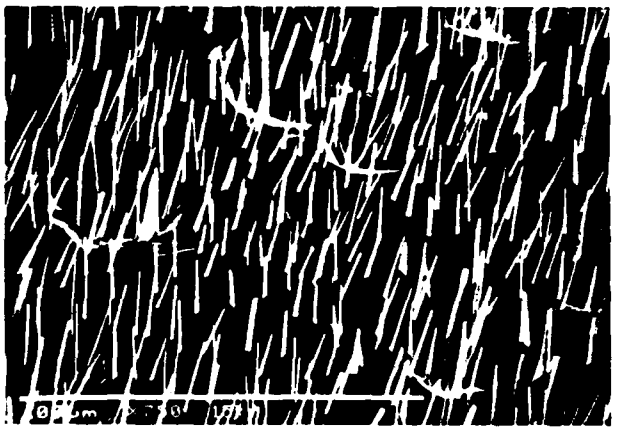


FIG. 1. Scanning electron micrograph of a transverse Si-$TaSi_2$ eutectic wafer after etching the surface Si to expose the rodlike shape of the $TaSi_2$ phase.

 0003-6951/86/501656-03$01.00

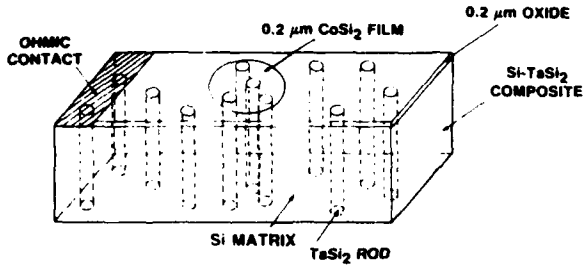


FIG. 2. Schematic diagram of the Si-$TaSi_2$ eutectic diode showing the $CoSi_2$ surface contact.

deposited Co film in a self-aligned process developed for Si integrated circuits.[11] The $CoSi_2$ provides a contact to the $TaSi_2$ rods while forming a Schottky barrier to the Si matrix. Ohmic contacts were formed at the edges of the wafers by deposition and alloying of a Au-Sb film. The device is schematically illustrated in Fig. 2.

Forward and reverse *I-V* characteristics of a typical eutectic device with a Si matrix having $N_d = 1.6\times 10^{15}$ cm^{3} are shown in Fig. 3. Based on the area of the $CoSi_2$ contact and the rod density, the device is calculated to contain 190 rods. For the 500-μm-thick wafer, assuming the length of each rod is equivalent to the wafer thickness, the total junction area of the diode is 3.6×10^{-3} cm^2. Since this corresponds to 30 times the area of the $CoSi_2$ contact to the Si matrix, and since $CoSi_2$ provides a slightly larger Schottky barrier to the Si than does $TaSi_2$ (0.64 eV vs 0.59 eV for thin-film junctions[12]), the contribution of the $CoSi_2$/Si junction to the *I-V* [and capacitance voltage(*C-V*)] characteristics is negligible.

Interpretation of the *I-V* characteristics may be based on the same thermionic emission diode equation used for planar junctions.[13] In this case

$$I = A_j A^* T^2 \exp(-q\phi_b/kT)[\exp(qV/nkT) - 1], \quad (1)$$

where A_j is the junction area, A^* is the Richardson constant equal to 120 A/cm K, ϕ_b is the Schottky barrier height, and T is temperature. As shown in Fig. 3, extrapolation of the linear portion of the forward and reverse current to 0 V yields a Schottky barrier height of 0.62 eV based on the total calculated $TaSi_2$/Si junction area. The value for these junctions prepared directly from the melt compares very well

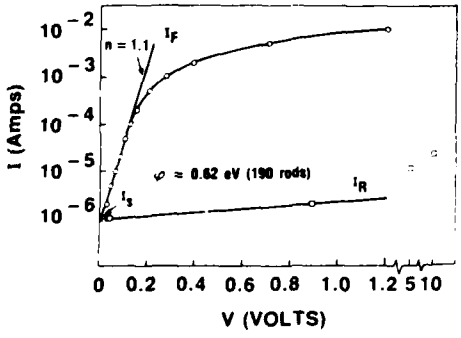


FIG. 3. Forward and reverse current-voltage characteristics of a typical *in situ* junction eutectic composite diode.

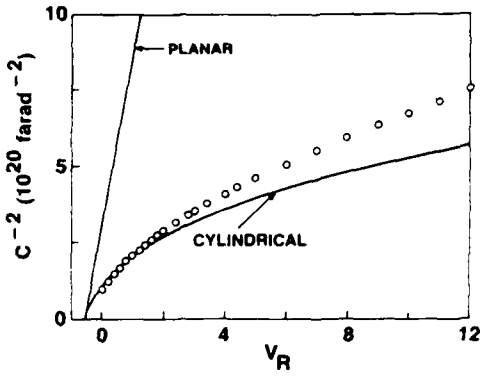


FIG. 4. Capacitance-voltage characteristics of a typical *in situ* junction eutectic composite diode. The solid lines show the calculated capacitance based on the planar and cylindrical junction models.

with the 0.59 eV determined for planar junctions formed by solid state diffusion. The diode is well behaved with an ideality factor $n = 1.10 \pm 0.05$. The large series resistance evident at higher forward voltages is due to the large distance from the diode to the ohmic contact at the edge of the wafer.

The reverse bias dependent capacitance of this eutectic diode was also investigated. Conventional planar diodes display a linear relationship between $1/C^2$ and V, which, as can be seen in Fig. 4, is clearly not the case for these eutectic diodes. In this case the cylindrical shape of the junctions, which tend to concentrate the electric field more than a planar junction, must be taken into account. Solution of Poisson's equation in cylindrical coordinates yields

$$\left[(r_0 + W)^2 - r_0^2 - 2(r_0 + W)^2 \ln\left(\frac{r_0 + W}{r_0}\right)\right] = \frac{-4\epsilon_s}{qN_d}(V_b + V_r), \quad (2)$$

where r_0 is the rod radius, W the depletion width, $V_b = \phi_b/q$, V_r is the applied reverse bias, and ϵ_s is the semiconductor dielectric constant. Due to field concentration this yields a smaller depletion width for a given reverse bias than a planar junction. Combining this with the relation for a parallel set of N_r coaxial capacitors of inner and outer radii, r_0 and $(r_0 + W)$,

$$C = \frac{2\pi\epsilon_s l N_r}{\ln[(r_0 + W)/r_0]} \quad (3)$$

yields

$$(V_b + V_r) = \frac{qN_d}{4\epsilon_s} r_0^2 \times\left[1 + \left(\frac{4\pi\epsilon_s l N_r}{C} - 1\right)\exp\left(\frac{4\pi\epsilon_s l N_r}{C}\right)\right], \quad (4)$$

where l is the rod length, assumed equal to the wafer thickness. Figure 4 shows the experimental data along with the *C-V* relationship calculated using the cylindrical junction expression in Eq. (4) and the measured device dimensions, the carrier concentration value from Hall data, and the Schottky barrier height determined from the *I-V* data. The calculated characteristic for a planar junction with the same

area, carrier concentration, and barrier height is included for comparison. Agreement of the measured capacitance, in both magnitude and voltage dependence, with the cylindrical junction model is considered to be quite good. The difference between the experimental and calculated data, particularly at large bias voltages, is probably due to depletion zone overlap. There is a distribution of interrod spacings in this material, and as the voltage is increased, the depletion layers of adjacent rods with interrod spacings equal to or less than twice the depletion width will begin to intersect. For instance, at a 10 V bias voltage, the depletion zone width around a 1.2-μm-diam rod is calculated to be 2.2 μm. Hence when the distance between two rods is less than 4.4 μm (the average spacing is 6.7 μm), some degree of depletion zone overlap or channel "pinch-off" would occur, causing a lower than calculated capacitance. Another possible reason for the overestimate of the capacitance is that some of the rods are faceted and elongated. These rods might have a depletion width that is underestimated by the cylindrical approximation.

In conclusion, we have shown that nearly ideal *in situ* multiple Schottky junction diodes can be fabricated from $TaSi_2$ eutectics. The Schottky barrier height of these grown-in junctions is comparable to $TaSi_2$/Si surface film junctions prepared by solid state diffusion processes. Capacitance measurements show that the depletion width can be controlled by bias voltage in good agreement with a cylindrical junction model. Demonstration of such well-behaved diodes and evidence that voltage-dependent depletion zones can be made comparable to the interrod spacing to produce a "pinch-off" condition opens many possibilities for novel device applications of this new class of electronic composite materials.

The authors wish to thank T. Middleton for his assistance in the growth of the composites and fabrication of the devices. The assistance of C. Coombs in device characterization is also gratefully acknowledged. Helpful discussions with J. Gustafson, B. Yacobi, and M. Alexander also contributed to this work. Research was sponsored by the Air Force Office of Scientific Research (AFSC), under contract F49620-86-C-0034. The United States Government is authorized to reproduce and distribute reprints for governmental purposes notwithstanding and copyright notation hereon.

[1]K. A. Jackson and J. D. Hunt, Trans. Metall. Soc. AIME **236**, 1129 (1966).
[2]B. Reiss and T. Renner, Z. Naturforsch **21A**, 546 (1966).
[3]D. E. Holmes, J. Electrochem. Soc. **128**, 859 (1981).
[4]A. Muller and M. Wilhelm, J. Phys. Chem. Solids **26**, 2021 (1965).
[5]N. J. Helbren and S. E. R. Hiscocks, J. Mater. Sci. **8**, 1744 (1973).
[6]B. M. Ditchek, J. Appl. Phys. **57**, 1967 (1985).
[7]B. M. Ditchek, J. Cryst. Growth **75**, 264 (1986).
[8]L. M. Levinson, Appl. Phys. Lett. **21**, 289 (1971).
[9]L. A. H. van Hoof and W. Albers, J. Appl. Phys. **52**, 3476 (1981).
[10]A. S. Yue and J. G. Yu, Proc. Fourth Intl. Conf. Composite Mater., ICCM-IV, Japan Society for Composite Materials, Tokyo, Japan, 1369 (1982).
[11]M. Tabasky, E. S. Bulat, B. M. Ditchek, M. A. Sullivan, and S. Shatas, in *Rapid Thermal Processing*, edited by T. Sedgwick, T. Seidel, and B. Y. Tsaur (Materials Research Society, Pittsburgh, PA, 1985), Proc. Mater. Res. Soc. **52**, 271 (1985).
[12]M. A. Nicolet and S. S. Lau, in *VLSI Electronics*, edited by N. Einspruch and G. Larrabee (Academic, New York, 1983), p. 330.
[13]S. M. Sze, *Physics of Semiconductor Devices* (Wiley, New York, 1969).

57/5 8

Appendix B

Characterization of Multiple *In Situ* Junctions in Si-$TaSi_2$ Composites By Charge-Collection Microscopy

Characterization of multiple *in situ* junctions in Si-$TaSi_2$ composites by charge-collection microscopy

B. G. Yacobi and B. M. Ditchek
GTE Laboratories, Waltham, Massachusetts 02254

(Received 8 January 1987; accepted for publication 16 February 1987)

The depletion zones of *in situ* metal-semiconductor junctions in a new class of electronic materials, Si-$TaSi_2$ eutectic composites, which are comprised of aligned $TaSi_2$ rods permeating a Si matrix, are characterized using charge-collection scanning electron microscopy. The increase in the depletion width of the individual Schottky junctions as a function of the reverse bias is measured. Results are in agreement with those predicted by a model of cylindrical junctions in a Si matrix. The observed overlap of the depletion zones around adjacent rods suggests possible field-effect transistor switch applications for this material.

Semiconductor-metal eutectic composite materials consist of an aligned array of metallic rods in a semiconductor matrix.[1-3] These systems, obtained by the directional solidification of eutectic mixtures, have promise as novel electronic materials because of the three-dimensional character of *in situ* rectifying junctions. For example, in a device application, the multiple vertical junctions of the semiconductor-metal eutectic composite could be used to control the flow of current through the interrod channels by the application of a reverse bias voltage in order to expand the depletion zones around the rods. The three-dimensional character of the junctions in the bulk device would enable the handling of much larger currents than are attainable with planar devices.

Semiconductor-metal composites have been largely ignored in the past, since it was *a priori* assumed that it would be very difficult to grow high quality electronic material for device applications. Recently, however, we have described the preparation, microstructure, and physical properties of various semiconductor-metal eutectic composites and have shown that composites of electronic quality can be obtained.[2-4] Among these systems, the Si-$TaSi_2$ composite appears the most promising.

The characterization of electronic properties of individual junctions is of great importance in evaluating device potential. Diode fabrication techniques and diode current-voltage (I-V) and capacitance-voltage (C-V) characteristics have already been reported for the Si-$TaSi_2$ system.[4] The purpose of the present work is to characterize the electronic properties of individual Schottky junctions in Si-$TaSi_2$ composites using the charge-collection scanning electron microscopy (or, as often referred to, electron beam induced current, EBIC) technique.[5] It is also shown that EBIC measurements can provide information on the continuity and alignment of the rods in a semiconductor-metal eutectic system.

The Si-$TaSi_2$ semiconductor-metal composite was obtained by directional solidification of the eutectic composition in a Czochralski crystal growth system.[3,4] The boules, grown at 20 cm/h, contain 2 vol. % metallic $TaSi_2$ rods oriented parallel to the growth direction and distributed in a grain-boundary-free Si matrix. The composites contain about 1.6×10^6 rods/cm^2 with an average rod diameter of 1.2 μm and an average interrod spacing of 7.9 μm.

Diodes fabricated for the EBIC measurements were prepared from wafers cut transverse to the growth direction of a phosphorus-doped boule. Hall-effect measurements were used to determine the carrier concentration. Most of the measurements were performed on a 500-μm-thick wafer with a carrier concentration $n\approx1.5\times10^{15}$ cm^{-3}. For studies of rod continuity and alignment, diodes were prepared from wafers ranging in thickness between 250 and 1250 μm. Ohmic contacts were made at the edges of the wafers by deposition and annealing of an Au-Sb film. Contacts to the silicide rods were made using a 0.2-μm-thick $CoSi_2$ film formed by rapid thermal annealing of a deposited Co film.[6] The $CoSi_2$ dot contact, 127 μm in diameter, provides an ohmic contact to the $TaSi_2$ rods, while providing a Schottky contact to the Si matrix. This Schottky interface, however, should not affect the charge collection measurements since our observations are performed on the opposite side of the wafer, i.e., the charge collection occurs far away from the $CoSi_2$ contact.

The EBIC technique is ideally suited for the electrical microcharacterization of the individual junctions in this composite. The schematic diagram of the specimen configuration during EBIC measurements is shown in Fig. 1. To block the diode current caused by reverse bias operation of

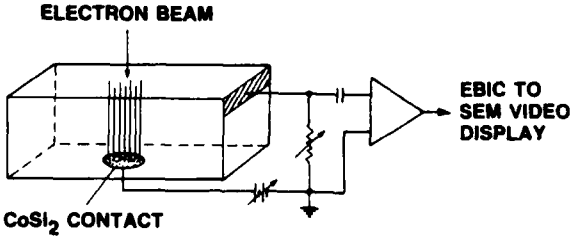


FIG. 1. Schematic diagram of the specimen configuration and the capacitor-coupled circuit for EBIC measurements.

 0003-6951/87/161083-03$01.00

the device, a capacitor-coupled detection method was used.

A secondary electron image (SEI) of the $TaSi_2$ rods intersecting the top surface of a polished wafer is shown in Fig. 2(a). The $TaSi_2$ rods are not perfectly circular in cross section, but are faceted. EBIC micrographs of the same area of a device without a bias and with a 5-V reverse bias, respectively, are shown in Figs. 2(b) and 2(c). The regions of high charge-collection efficiency outline the depletion zone surrounding the rod. Despite the faceting of the $TaSi_2$/Si interface, the depletion zones are approximately circular in cross section. As expected, with the application of the reverse bias voltage, the depletion zones expand and eventually overlap [Fig. 2(c)].

The width of the depletion zone was measured from EBIC line scans across the junction. Since the boundary of the depletion zone is not marked by an abrupt change in the collection current, the zone boundary was defined as the point where the EBIC signal fell to 3/4 of its maximum value. This definition could introduce up to 35% error in the measurement of the unbiased depletion width. This error determination is based on the analysis of the slope of the initial EBIC signal decay. For conventional planar devices, EBIC line scans can be calibrated using capacitance measurements of the depletion width of the same diode.[7] In the case of these composite diodes, modeling the capacitance as an array of coaxial capacitors (as opposed to parallel plate capacitors) yields a depletion zone of 0.49 μm assuming that all rods are ideal cylinders with the average rod diameter of 1.2 μm.[4] This compares favorably with the measured unbiased depletion width of about 0.5 ± 0.2 μm using our definition of the depletion zone boundary. However, since the size and shape of the rods can deviate considerably from this model, the capacitance measurement is not used for calibration but only to show a reasonable agreement.

In these measurements, the size of the electron beam excitation volume was kept smaller than the measured depletion width. This was achieved by minimizing the electron-beam energy. In all measurements, 5- and 10-keV electron beams of about 1 nA were used. The excitation range for a 5-keV electron beam, for example, is about 0.3 μm, which is less than the depletion zone widths reported here. It should be noted that at low electron beam energies, the effect of surface recombination may become important. However, the electron beam energies used in these measurements are still sufficient to produce largely a bulk effect.

Figure 3 shows the dependence of the depletion width on the reverse bias voltage measured at a 1-μm-diam $TaSi_2$ rod (see insert). This particular rod was isolated from other rods by a distance greater than the maximum depletion width measured and, in addition, it had nearly perfect cylindrical symmetry. The data in Fig. 3 are compared to the calculated dependence of the depletion zone width as a function of the reverse bias derived from a solution to Poisson's equation for both planar and cylindrical junctions using $n = 1.5 \times 10^{15}\,\mathrm{cm}^{-3}$, the value measured for this wafer using the Hall effect. For a metallic cylinder of radius r_0 embedded in a semiconductor, the solution of Poisson's equation in cylindrical coordinates yields an expression which relates the depletion width to the reverse bias voltage

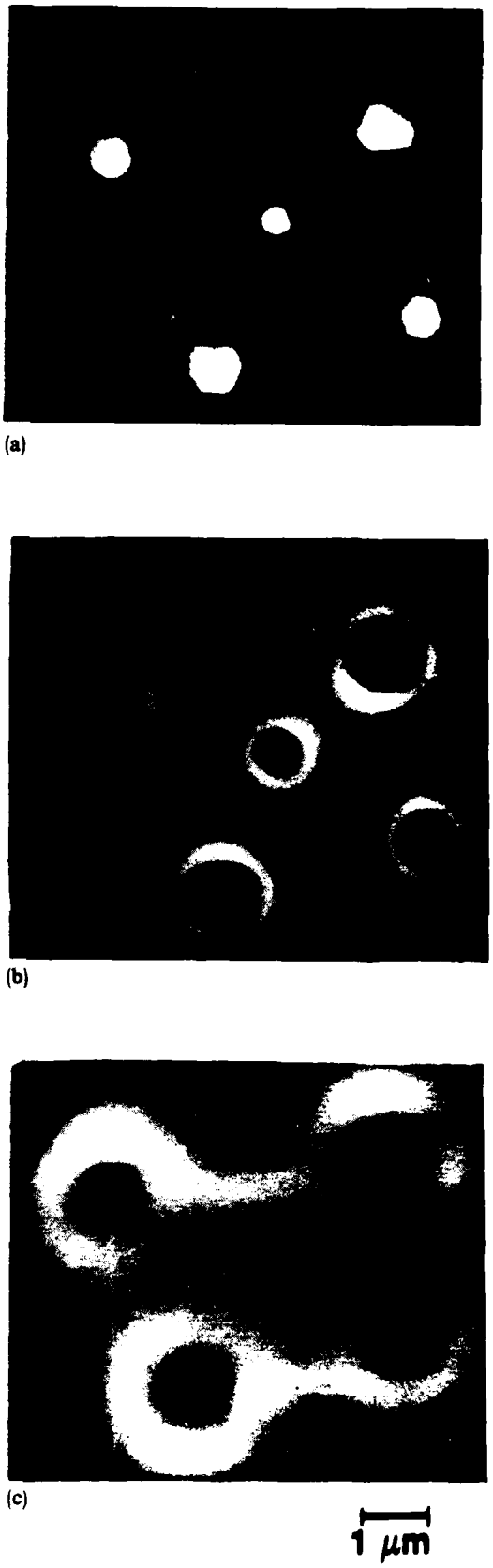


FIG. 2. SEM micrographs of the portion of the Si-$TaSi_2$ eutectic diode. (a) Secondary electron image (SEI) of $TaSi_2$ rods embedded in a Si matrix. (b) Corresponding EBIC image (unbiased). (c) EBIC image at a reverse bias of 5 V. In all cases the electron beam energy is 10 keV and the SEM electron beam current is about 1 nA.

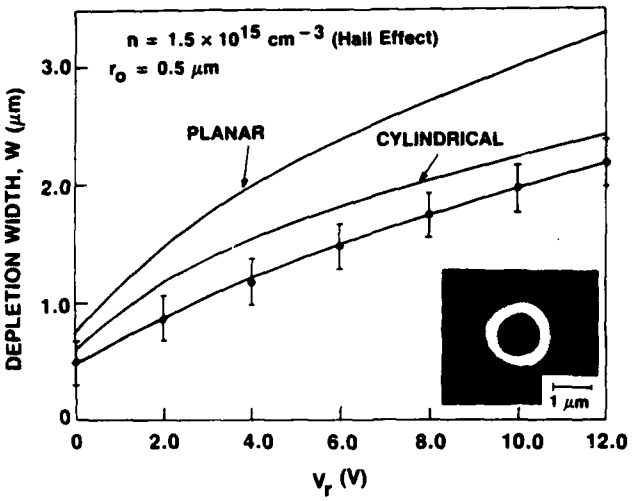


FIG. 3. Depletion width as a function of the reverse bias. The solid lines correspond to the depletion widths calculated from the planar and cylindrical junction models. The solid dots correspond to experimental data obtained from a junction shown (unbiased) in the insert. In this case, the electron beam energy is 5 keV.

$$\left[(r_0 + W^2) - r_0^2 - 2(r_0 + W)^2 \ln\left(\frac{r_0 + W}{r_0}\right)\right] = \frac{-4\epsilon_s}{qn}(V_b + V_r), \quad (1)$$

where r_0 is the rod radius, W is the depletion width, and $V_b = \phi_b/q$, where ϕ_b is the Schottky barrier height, V_r is the applied reverse bias, and ϵ_s is the dielectric constant of the semiconductor. For a given bias voltage and carrier concentration, the cylindrical junction model predicts a smaller depletion zone width than the planar junction model due to field concentration.

The experimental points fall below depletion width values calculated from the cylindrical junction model. An approximate fit to the points corresponds to $n \simeq (2.2 \pm 0.6) \times 10^{15}\,\mathrm{cm}^{-3}$, which averages about 50% higher than the Hall carrier concentration. However, since depletion zones surrounding the rods are expected to cause a small underestimate of the Hall-effect carrier concentration,[2,8] the agreement between the experimental data and those calculated using the cylindrical junction model is considered to be good. This would also indicate that the doping concentration is fairly uniform, at least in the vicinity of up to several microns away from the rod. These results are in accord with previous capacitance-voltage analysis of these diodes which showed the good agreement between capacitance measurements and those calculated on the basis of a cylindrical junction model.[4]

In this composite, there is a distribution of interrod spacings. Thus, as a function of the reverse bias, in regions of the diode with interrod spacings of twice (or less) the depletion width, depletion zone overlap will occur. For example, at a 5-V reverse bias voltage, the depletion width around a 1.0-μm-diam rod is 1.2 μm, and when the distance (from boundary to boundary) between adjacent rods is less than 2.4 μm, depletion zone overlap will occur. Figure 2(c) shows a cluster of rods for which the interrod spacings are small enough so that a 5-V reverse bias causes the depletion zone overlap. Larger reverse bias voltages or larger unbiased depletion zone widths (i.e., lower carrier concentrations) will be required for the depletion zone overlap of adjacent rods with larger interrod spacings.

In addition to electronic characterization, EBIC analysis of these composites also provides information on the continuity and alignment of the rods. EBIC measurements on wafers with various thicknesses (up to 1250 μm) indicate that the rods are continuous through all the wafers, including the 1250-μm-thick wafer. In addition, the maximum divergence of the rods, measured from a comparison of the total diameter of the $CoSi_2$ contact and the spread between rods in EBIC measurements on the opposite side of the wafer, was determined to be about 6°. These observations provide encouragement for using thick wafers in high-power field-effect transistor (FET) device applications. In addition, these studies show that the EBIC technique can be effectively used for measuring the length and divergence of the rods in the composite.

In summary, we have demonstrated that the depletion zones of multiple *in situ* junctions in Si-$TaSi_2$ composites can be manipulated with the reverse bias voltage in agreement with a cyclindrical junction model. Charge-collection microscopy has provided direct evidence for the overlap of depletion zones around adjacent rods and has demonstrated continuity of the rods through thick wafers. The results indicate that this material has promise in high-power FET switch applications.

The authors would like to thank T. Middleton for assistance in the crystal growth and preparation of the samples. Helpful discussions with M. Levinson and J. Gustafson are also gratefully acknowledged. This work was sponsored in part by the Air Force Office of Scientific Research under contract F49620-86-C-0034 and by the Office of Naval Research under contract N00014-86-C-0595. The United States Government is authorized to reproduce and distribute reprints for governmental purposes notwithstanding any copyright notation hereon.

[1] N. J. Helbren and S. E. R. Hiscocks, J. Mater. Sci. **8**, 1744 (1973).
[2] B. M. Ditchek, J. Appl. Phys. **57**, 1967 (1985).
[3] B. M. Ditchek, J. Cryst. Growth **75**, 264 (1986).
[4] B. M. Ditchek and M. Levinson, Appl. Phys. Lett. **49**, 1656 (1986).
[5] H. J. Leamy, J. Appl. Phys. **53**, R51 (1982).
[6] M. Tabasky, E. S. Bulat, B. M. Ditchek, M. A. Sullivan, and S. Shatas, in *Rapid Thermal Processing*, Proceedings of Materials Research Society, Vol. 52, edited by T. Sedgwick, T. Seidel, and B.-Y. Tsaur, p. 271 (1985).
[7] J. D. Schick, in *Scanning Electron Microscopy/1981*, edited by O. Johari (SEM, Chicago, IL), Vol. I, p. 295.
[8] W. T. Read, Jr., Philos. Mag. **46**, 111 (1955).

63 / 64

Appendix C

EBIC Characterization of Multiple *In Situ* Three-Dimensional Junctions in Silicon

Inst. Phys. Conf. Ser. No. 87: Section 11
Paper presented at Microsc. Semicond. Mater. Conf., Oxford, 6–8 April 1987

EBIC characterization of multiple *in situ* three-dimensional junctions in silicon

B G Yacobi and B M Ditchek

GTE Laboratories, Waltham, Massachusetts 02254

ABSTRACT: The electron-beam-induced current (EBIC) mode of the scanning electron microscope has been used to characterize the individual semiconductor-metal junctions in Si–$TaSi_2$ eutectic composites. These materials consist of aligned $TaSi_2$ rods permeating a Si matrix. The EBIC results show that depletion zones of the *in situ* multiple Schottky junctions can be manipulated with a reverse bias voltage in agreement with the cylindrical junction model. The analysis has shown that the carrier concentration values derived from EBIC measurements provide a better estimate of the carrier concentration in the vicinity of a junction than do Hall effect measurements. EBIC observations have also revealed the presence of microplasma sites which are most probably associated with dislocations observed in TEM studies.

1. INTRODUCTION

A new class of electronic materials, semiconductor-metal eutectic composites, consist of an aligned array of *in situ* metallic rods permeating a semiconductor matrix. These systems are obtained by the directional solidification of eutectic mixtures. The resulting three-dimensional arrays of rectifying junctions suggest several novel device applications such as high-power switches and photodiode devices.

Until recently, semiconductor-metal composites were largely ignored. Although several semiconductor-metal composite systems were reported — for example, Ge- and Si-based (Helbren and Hiscocks 1973) and GaAs-based (Reiss and Renner 1966) eutectic systems — these Bridgman-grown composites had polycrystalline semiconductor matrices and were unsuitable for most electronic device applications. The recent availability of Czochralski-grown composites with single-crystal semiconductor matrices (Ditchek 1986, Ditchek and Levinson 1986, Yacobi and Ditchek 1987) has renewed interest in the electronic properties of this class of materials.

The transport properties of eutectic composites will be affected by the unique microstructure of the material and by the presence of depletion zones in the interrod channels of the matrix. For device applications, the transport and junction properties of these materials must be delineated and understood. The EBIC technique is ideally suited for the characterization of the individual junctions in such systems. This work presents the results of an EBIC analysis of Si–$TaSi_2$ composites.

2. EXPERIMENTAL

The composite materials for this study were prepared by directional solidification of the eutectic composition of Si–5.5 wt.% Ta using a Czochralski crystal growth technique (Ditchek 1986, Ditchek and Levinson 1986). The material was grown at 20 cm/hr and contains 1.6×10^6 $TaSi_2$ rods/cm^2 oriented parallel to the growth direction and distributed irregularly in a single-crystal Si matrix. The $TaSi_2$ phase constitutes 2 vol.% of the composite. The average rod diameter and interrod spacing are 1.2 μm and 7.9 μm, respectively. The melt was doped with phosphorus to yield a carrier concentration on the order of 10^{15} cm^{-3}.

Diodes were prepared from wafers (500 μm thick) cut transverse to the growth direction. Contacts to the $TaSi_2$ rods were made by rapidly annealing a deposited Co film to form $CoSi_2$. The 0.2 μm thick $CoSi_2$ film provides a Schottky contact to the Si and an ohmic contact to the $TaSi_2$ rods. The 127 μm diameter contact dot contains about 200 rods. The EBIC measurement arrangement is shown schematically in Figure 1. A capacitor-coupled detection method was used to block the diode current caused by the application of the reverse bias to the diode.

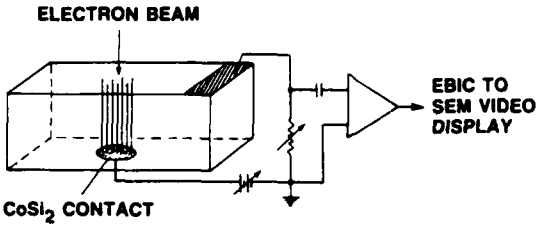


Figure 1. Schematic diagram of the specimen and the circuit for EBIC measurements.

The measurements of the depletion zone widths were performed with a 5-keV electron beam of about 1 nA. The excitation range in this case is about 0.3 μm and is smaller than the depletion zone widths of interest. Although for small excitation ranges surface recombination may become important, the present experimental conditions are expected to produce largely a bulk effect.

3. RESULTS AND DISCUSSION

A secondary electron image of the $TaSi_2$ rods intersecting the surface of a polished wafer is displayed in Figure 2(a). A majority of the rods, in cross section, are faceted with a small percentage exhibiting a triangular shape or an elongated shape with rounded ends. In the EBIC image in Figure 2(b), the bright regions around the rods outline the depletion zones. Despite the faceting of the rods, the depletion zones are nearly circular. The depletion zone around one rod is not visible in the EBIC mode in this micrograph. As will be discussed later, this is caused by enhanced recombination at defects surrounding some of the rods.

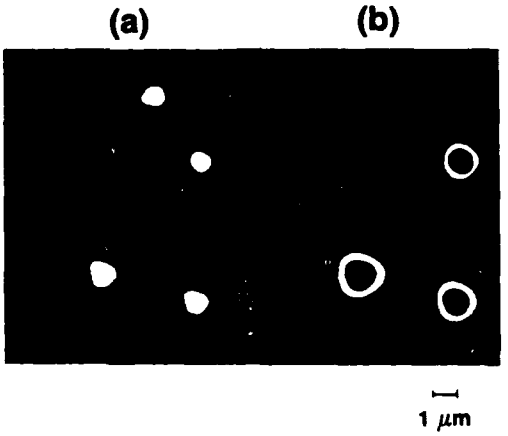


Figure 2. (a) Secondary electron image of $TaSi_2$ rods embedded in the Si matrix, and (b) corresponding EBIC image (unbiased) of the portion of the Si-$TaSi_2$ eutectic diode.

It is expected that the application of a reverse bias voltage to the rods will cause the depletion zones to expand and eventually overlap. This effect is demonstrated in Figure 3 for a portion of the diode. The micrograph series clearly shows that with the application of the reverse bias of 10 V, the interrod channels are *pinched-off*, i.e., blocked for the transconductance of majority carriers. The ability to manipulate the extent of the depletion zones by the application of a nominal bias voltage is attractive for high-power switching device applications.

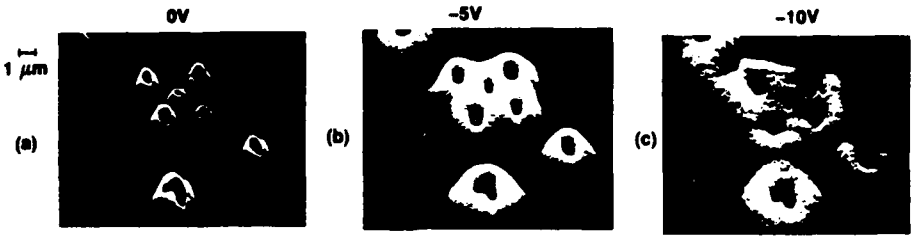


Figure 3. Y-modulation EBIC images of the portion of the Si-$TaSi_2$ eutectic diode: (a) unbiased, (b) at a reverse bias of 5 V, and (c) at a reverse bias of 10 V. In all cases the electron-beam voltage is 10 kV and the SEM electron-beam current is about 1 nA.

The depletion zone width (W) as a function of the reverse bias voltage (V_r) has been obtained from EBIC line scans across the individual junctions. Because the depletion zone boundary is not marked by an abrupt change in the charge-collection current, it is necessary to adopt a convention for defining the depletion zone boundary for comparison purposes. This can be done by using capacitance-voltage measurements of the depletion zone width to *calibrate* the EBIC measurement. An unbiased depletion zone width of 0.49 μm was obtained from capacitance measurements by assuming that all rods are perfect cylinders and by treating the system as an array of coaxial capacitors (Ditchek and Levinson 1986). This value corresponds to the point at which the EBIC signal falls to 0.75 of its maximum value. It should be emphasized that this *calibration* value is appropriate for this particular case only, and it should not be taken as a general calibration factor for the measurement of the depletion zones in other devices.

EBIC measurements of the depletion zone width have been used to determine the carrier concentration (n) in the silicon matrix. This analysis was performed by fitting the theoretically predicted depletion zone widths (W) as a function of the reverse bias voltage (V_r) to the data extracted from EBIC measurements. The expression used in the analysis was derived from the solution to Poisson's equation in cylindrical coordinates:

$$\left[(r_o + W)^2 - r_o^2 - 2(r_o + W)^2 \ln\left(\frac{r_o + W}{r_o}\right)\right] = \frac{-4\epsilon_s}{qn}(V_b + V_r) \qquad (1)$$

where r_o is the rod radius, W is the depletion width, $V_b = \phi_b/q$ (ϕ_b is the Schottky barrier height), and ϵ_s is the dielectric constant of the semiconductor. Figure 4 presents the results. The solid and dashed lines without experimental points correspond to the $W(V_r)$ relationship calculated from Eq. (1) using the carrier concentrations (n_H) obtained from Hall effect measurements on two samples with different carrier concentrations. The experimental points correspond to values derived from the EBIC line scan measurements. The fitted curves were calculated from Eq. (1) by using the carrier concentration as an adjustable parameter. Concentrations denoted n_{EBIC} resulted in the best fit. As can be deduced from this figure, the agreement between n_H and n_{EBIC} for a sample with higher carrier concentration (dashed lines) is good. However for a sample with lower carrier concentration (solid lines), the discrepancy between n_H and n_{EBIC} is too large to be explained by errors in either the Hall effect or EBIC measurements. Rather, this discrepancy is a manifestation of the influence of depletion zone size on transport properties. As the carrier concentration is decreased, the unbiased depletion zones expand and lead to a narrowing of the interrod channels. This impedes transport through the interrod channels and results in an underestimation of carrier concentrations extracted from Hall effect

measurements. The EBIC measurements, however, do not depend on transport through the interrod channels. Thus, EBIC measurements can give the true carrier concentrations around the rods. The excellent fit to the data obtained using Eq. (1) indicates that the carrier concentration is fairly uniform in the vicinity of the rods. A detailed discussion of the depletion-zone-limited transport in these materials will appear elsewhere (Ditchek, Yacobi and Levinson, to be published).

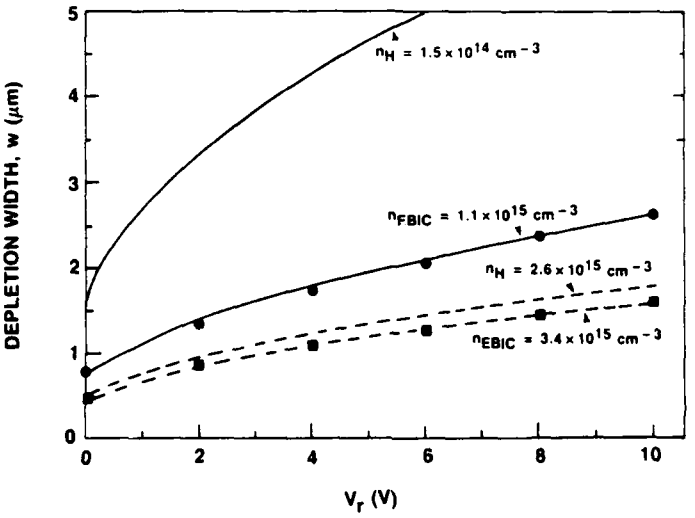


Figure 4. Depletion widths as a function of the reverse bias. Two sets of solid and dashed lines correspond to two samples with different carrier concentrations. Curves are calculated using Eq. (1) and the experimental points were derived from EBIC measurements. n_H indicates the carrier concentration derived from the Hall effect measurements, while n_{EBIC} corresponds to the carrier concentrations derived by fitting the EBIC experimental points to the calculated curves.

In the unbiased case, only about 70% of the rods are visible in the EBIC mode (see Figure 5). With the application of a reverse bias voltage, however, the expansion of the depletion zones is accompanied by a gradual increase in the number of rods observable in the EBIC image (Figure 5) and by the formation of microplasma sites in localized regions of the diode. In semiconductor devices, defects located in the depletion zone may act as sites for local electric field enhancement which lead to an increase in the EBIC signal. Such microplasma sites usually reveal regions of premature breakdown and may be caused, for example, by mechanical scratches, surface contamination, inclusions, dislocations, and/or stacking faults. The detailed correlation of the EBIC images of individual unbiased and biased junctions with transmission electron microscope (TEM) observations suggests that the most plausible cause for the microplasma sites in these composites is the presence of dislocation clusters (with density of up to 10^7 cm^{-2}) around the semiconductor-metal interfaces in some regions of the sample (see Figure 6).

In most cases, sites that have generated microplasmas under a bias have also exhibited low unbiased EBIC signals because of the high recombination rates associated with the defects. For example, the case illustrated in Figure 7 shows a microplasma site being generated as the reverse bias voltage is applied. It should be noted that this was the only

case in which such a low reverse bias voltage led to a pronounced effect. Typically, voltages on the order of 5 to 10 V are necessary to observe the microplasma sites (see Figure 5). Also, recently prepared Si–$TaSi_2$ composites have exhibited very few microplasma sites at reverse bias voltages of up to 30 V.

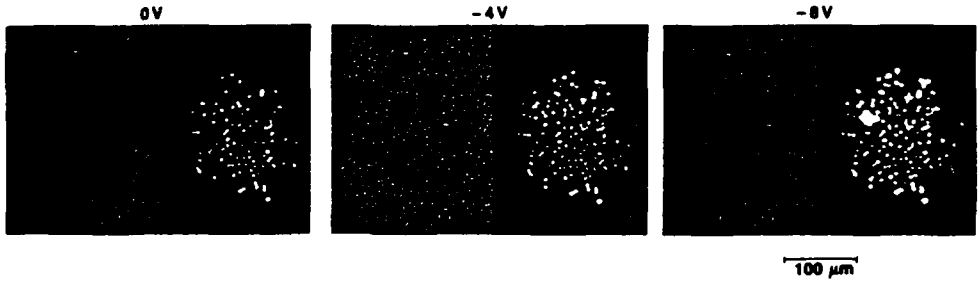


Figure 5. Secondary electron images and corresponding EBIC images of a diode as a function of the reverse bias voltage.

Figure 6. Bright field TEM image of a heavily dislocated region of the composite sample.

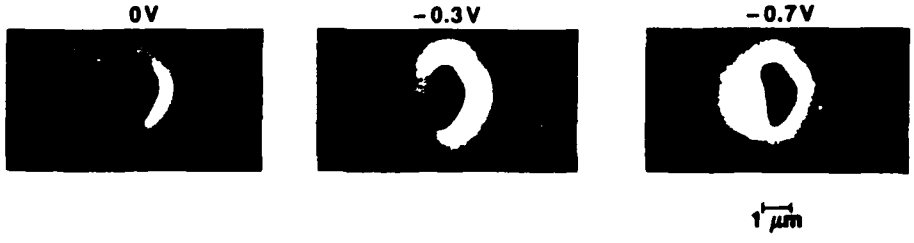


Figure 7. Unbiased and reverse-biased EBIC images of a $TaSi_2$ rod in a Si matrix.

CONCLUSIONS

The EBIC observations have demonstrated that the depletion zones of *in situ* semiconductor-metal junctions in Si–$TaSi_2$ composites can be manipulated with the application of the reverse bias voltage. The EBIC measurements of the dependence of the depletion width as a function of the reverse bias voltage have been used to derive the carrier concentration in the Si matrix. It has been shown that the EBIC analysis gives more reliable estimates of carrier concentration than do Hall effect measurements in cases exhibiting depletion-zone-limited transport. The results suggest that this material, with its unique three-dimensional array of rectifying junctions, has promise in a variety of device applications.

ACKNOWLEDGMENTS

The authors thank T. Middleton for assistance in the growth and sample preparation. Helpful discussions with J. Gustafson and M. Levinson are also gratefully acknowledged. This research was sponsored in part by the Air Force Office of Scientific Research under contract F49620-86-C-0034 and by the Office of Naval Research under contract N00014-86-C-0595. The U.S. Government is authorized to reproduce and distribute reprints for governmental purposes notwithstanding any copyright notation hereon.

REFERENCES

Ditchek B M 1986 J. Cryst. Growth 75 264

Ditchek B M and Levinson M 1986 Appl. Phys. Lett. 49 1656

Helbren N J and Hiscocks S E R 1973 J. Mater. Sci. 8 1744

Reiss B and Renner T 1966 Z. Naturforsch. 21A 546

Yacobi B G and Ditchek B M 1987 Appl. Phys. Lett. 50 1083

Appendix D

Capacitance Spectroscopy of Si-$TaSi_2$ Eutectic Composite Structures

Capacitance spectroscopy of Si-$TaSi_2$ eutectic composite structures

M. Levinson, B. M. Ditchek, and B. G. Yacobi
GTE Laboratories, Inc., 40 Sylvan Road, Waltham, Massachusetts 02254

(Received 23 March 1987; accepted for publication 30 April 1987)

The Si matrix phase of directionally solidified Si-$TaSi_2$ eutectic composite structures has been characterized by deep level capacitance transient spectroscopy, using the grown-in metal-semiconductor junctions. The Si is found to be of high quality. No electrically active Ta was detected with a minimum experimental sensitivity of $\sim 6\times 10^{11}$ cm^{-3}. Some samples exhibited one of two defect states having electron emission activation energies of 0.36 and 0.65 eV. These states appear to be associated with dislocations.

Directionally solidified semiconductor-metal eutectic composite structures form an interesting new class of electronic materials. These composites can be grown so as to contain a quasi-regular array of parallel metallic rods embedded in a single-crystal semiconductor matrix. The two phases can form rectifying junctions, and with the proper contacts, Schottky diodes may be fabricated. Well behaved diodes, formed using the grown-in metal-semiconductor junctions of a Si-$TaSi_2$ composite, have recently been demonstrated.[1]

Potential electronic and optoelectronic applications of these composites will be dependent on the quality of both the metal-semiconductor junctions and the semiconducting matrix material. The junctions of our Si-$TaSi_2$ composites have been shown to behave as nearly ideal Schottky barriers.[1] In this letter, we show that the Si matrix material of such composite diodes can be characterized using deep level capacitance transient spectroscopy (DLTS) with the grown-in junctions. This technique allows the detection of any electrically active lattice defects and impurities, such as Ta, which might be expected in these materials and which would degrade the electronic properties of the Si. We also present an analysis of capacitance transient methods for cylindrical junction geometries, and show that excellent data can be obtained.

The eutectic composites used in this study were of P-doped Si-$TaSi_2$ grown by a Czochralski method.[2] The $TaSi_2$ rods were $\sim 1\,\mu$m in diameter with an average interrod spacing of $\sim 8\,\mu$m. 500-μm-thick wafers were cut perpendicular to the rods. A $CoSi_2$ metallization was used to contact the rods while maintaining a rectifying barrier to the Si, as previously described.[1] In this process Co was deposited and reacted in openings in an oxide film formed by a 1000 °C, 60 min anneal. A schematic diagram of the device is shown in Fig. 1. Contacts of 1.3×10^{-4} cm^2 produced devices containing ~ 200 rods. The total area of semiconductor-rod interface was 3.7×10^{-3} cm^2, or about 30 times that of the $CoSi_2$ contact, so the DLTS signal was predominantly due to the depletion regions surrounding the rods. The capacitance-voltage response of these diodes was in good agreement with that expected for cylindrical junctions with a free-electron concentration $n = 2\times 10^{15}$ cm^{-3}, as verified by Hall-effect measurements.[1]

For these devices, an analysis of capacitance transients must take into account the cylindrical junction geometry. Solving Poisson's equation in cylindrical coordinates, and using the expression for the capacitance of coaxial cylinders, we obtain[1,3]

$$V_B + V_R = \frac{qr^2(N_D - N_T)}{4\epsilon_s} \times \left[1 + \left(\frac{4\pi\epsilon_s n_r l}{C} - 1\right)\exp\left(\frac{4\pi\epsilon_s n_r l}{C}\right)\right], \quad (1)$$

where V_B is the built-in junction potential, V_R is the applied reverse bias, q is the electronic charge, r and l are the rod radius and length, N_D is the effective shallow dopant concentration, N_T is the concentration of traps occupied by majority carriers, n_r is the number of rods accessed by the contact, ϵ_s is the semiconductor permittivity, and C is the capacitance. It is apparent that, given a constant bias voltage, C is not a simple function of the trap concentration. However, if the capacitance is held fixed, then $V_B + V_R$ is just proportional to $N_D - N_T$, so that

$$N_T(t) = \frac{N_D}{V_B + V_R^0}\,\Delta V_R(t), \quad (2)$$

where V_R^0 is the quiescent reverse bias and $\Delta V_R(t)$

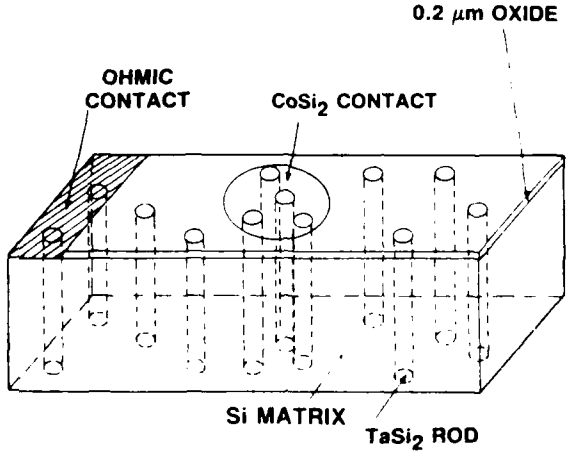


FIG. 1. Schematic diagram of the eutectic composite diode.

 0003-6951/87/261906-03$01.00

$= V_R^0 - V_R(t)$. Therefore, if the DLTS measurement is implemented in the constant capacitance mode, ΔV_R accurately reflects the exponential trap emptying transient and the data may be interpreted in the normal manner.

Constant capacitance DLTS spectra were measured for eleven diodes on two wafers from the same boule. Representative spectra are shown in Fig. 2. Two diodes showed no detectable signals [Fig. 2(a)]. The minimum experimental sensitivity then gives an upper limit for the concentration of deep states in the upper half band gap as $N_t \lesssim \sim 6\times 10^{11}$ cm^{-3}. Four diodes yielded one DLTS peak E(0.36 eV) [Fig. 2(b)] with an electron emission activation energy of 0.36 eV as shown in Fig. 3. The apparent concentrations of this defect state varied between 3.2×10^{12} and 1.7×10^{13} cm^{-3}. However, variation of the filling pulse width showed that this feature was actually a superposition of two peaks with similar activation energies, but different electron capture cross sections, 1.1×10^{-16} cm^2 and $\sim 4\times 10^{-19}$ cm^2.

The other five diodes all showed a different DLTS peak [Fig. 2(c)] with an emission activation of 0.65 eV (Fig. 3). The electron capture cross section was measured to be 7.1×10^{-17} cm^2 and apparent concentrations were in the range 1.3–2.4×10^{14} cm^{-3}.

The fact that different defect states were observed in different diodes, and that none was seen in some, is an indication that these defects are inhomogeneously distributed, and that in some regions the concentrations are undetectably small. Such an inhomogeneous distribution would not be

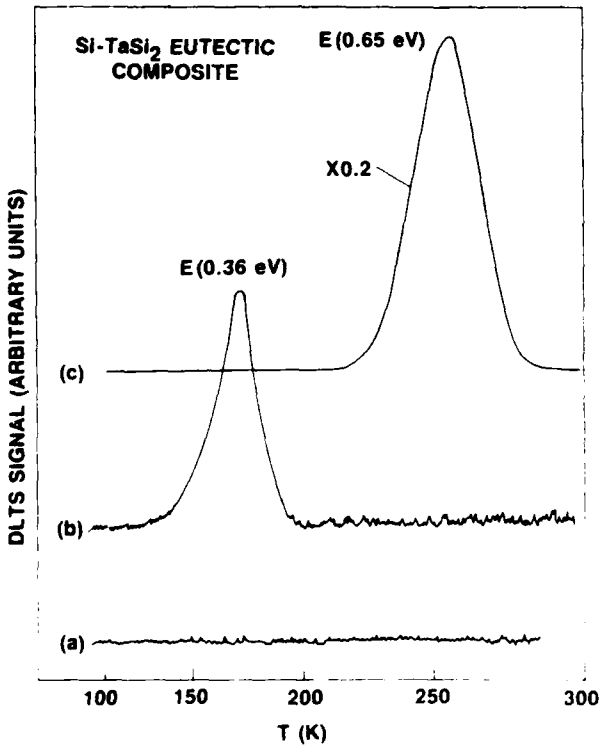


FIG. 2. DLTS spectra. Rate window $\tau_{DLTS} = 30$ ms.

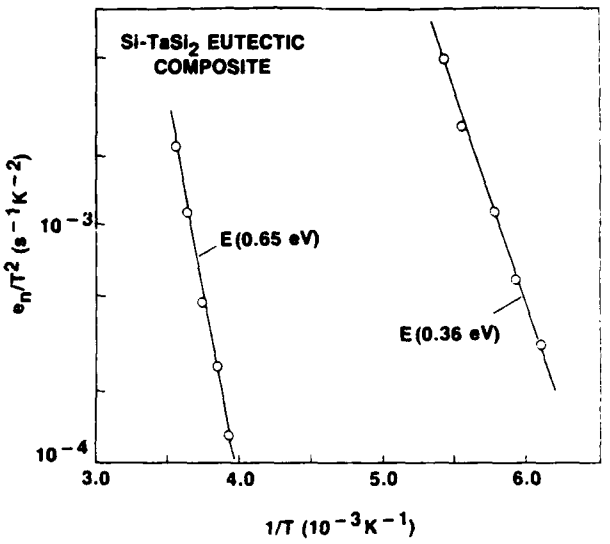


FIG. 3. Arrhenius plots of emission rate data for peaks E(0.36 eV) and E(0.65 eV).

expected for substitutional impurities present in the melt during crystal growth. The major electrically active impurity expected to be found in the Si would be Ta. However, neither of the observed defect states corresponds to those reported for Ta (Ref. 4): two donor states at $E_c - 0.23$ eV and $E_c - 0.47$ eV. We may conclude that the concentration of electrically active Ta in the Si matrix is less than $\sim 6\times 10^{11}$ cm^{-3}, and that this is likely also true for all other impurities.

The defect states found in this material are probably the result of an inhomogeneous distribution of extended defects. Electron beam induced current experiments have shown inhomogeneously distributed areas of enhanced electron-hole recombination in this material.[5] These regions probably contain high dislocation densities. Preliminary examination by transmission electron microscopy has in fact revealed dislocation-rich areas in the Si. Furthermore, the presence of defect states E(0.36 eV) and E(0.65 eV) is in good agreement with the dominant states reported to be associated with plastic deformation induced dislocations in Si. These have electron emission activation energies of 0.38 and 0.68 eV (Ref. 6).

In conclusion, capacitance transient spectroscopy measurements have been made on the Si matrix material of Si-$TaSi_2$ eutectic composites by means of the *in situ* metal-semiconductor junctions. The Si was found to be of high electronic quality. No electrically active Ta was detected above the sensitivity limit of $\sim 6\times 10^{11}$ cm^{-3}. Inhomogeneous concentrations of defects were observed with electron emission activation energies of 0.36 and 0.65 eV. These appear to be associated with dislocations present in the Si. This material, with its unique junction geometry, is therefore a promising one for many novel electronic devices, although some reduction in dislocation densities may be desirable for those involving minority carriers.

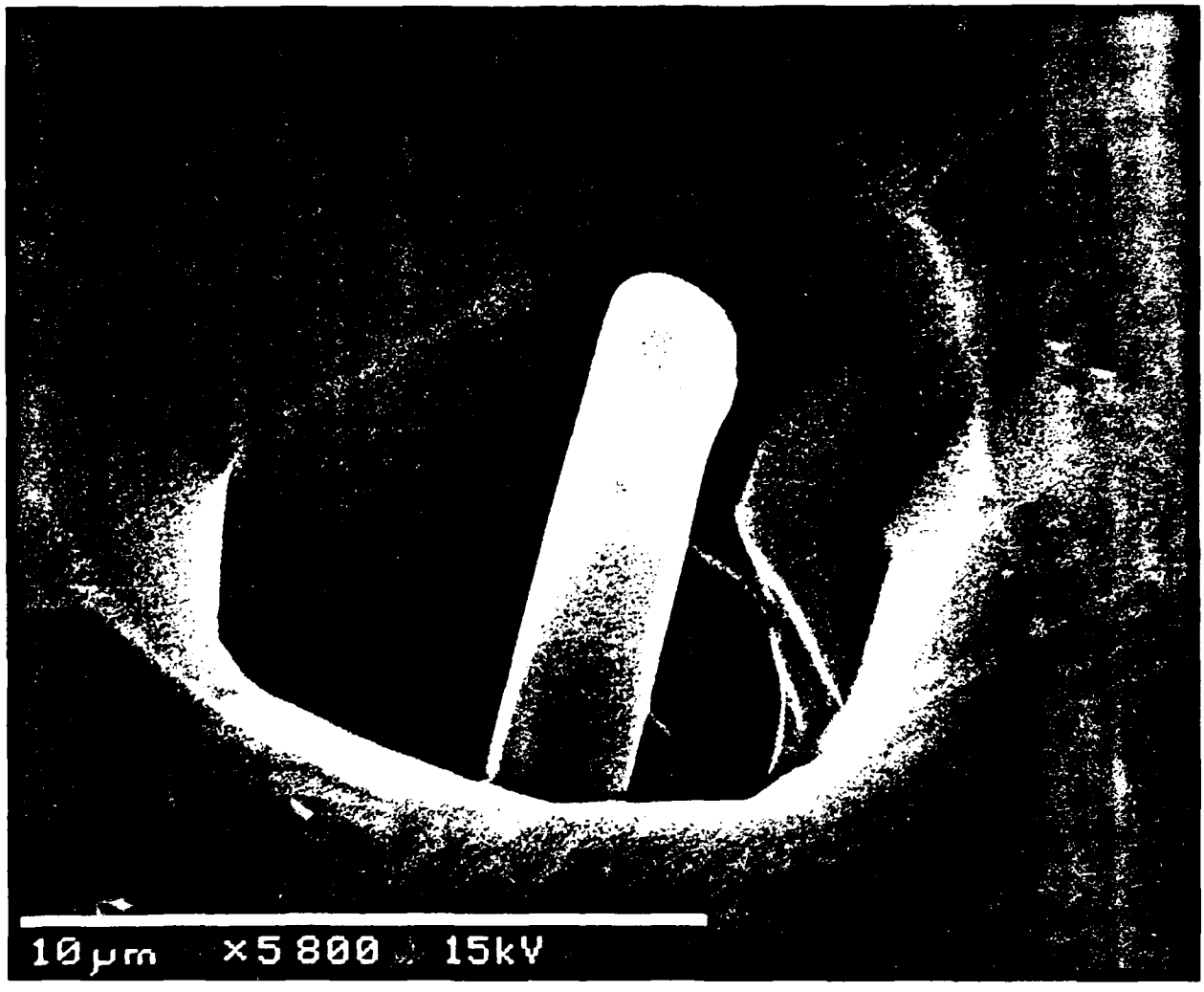
This work was sponsored in part by the Air Force Office of Scientific Research under contract F49620-C-0034; and by the Office of Naval Research under contract N00014-86-C-0595.

[1]B. M. Ditchek and M. Levinson, Appl. Phys. Lett. **49**, 1656 (1986).
[2]B. M. Ditchek, J. Cryst. Growth **75**, 264 (1986).
[3]T. P. Lee and S. M. Sze, Solid-State Electron. **10**, 1105 (1967).
[4]K. Miyata and C. T. Sah, Solid-State Electron. **19**, 611 (1976).
[5]B. G. Yacobi and B. M. Ditchek, Appl. Phys. Lett. **50**, 1083 (1987).
[6]L. C. Kimerling and J. R. Patel, Appl. Phys. Lett. **34**, 73 (1979).

Appendix E

Semiconductors with Built-In Junctions

Semiconductors with Built-In Junctions



by B. M. Ditchek/B. G. Yacobi/M. Levinson

semiconductors

Essentially all electronic devices begin the same way—with a simple, semiconducting substrate. The substrate is a uniform block of material upon which junctions are built. Typically, junctions—the nonuniform section of the material associated with the internal electric field through which electronic devices operate—are built either into the surface of the substrate or built on top of the surface. Thus, the bulk of the substrate contains no junctions and is essentially inactive. It simply acts as a carrier for the active part of the device at the substrate surface.

Over the years, researchers have successfully worked within this framework to advance the science of electronics. Indeed, it is the basis of all of today's electronic and optoelectronic devices. Nevertheless, such a framework is also restricting.

Could new, improved devices be fabricated from substrates that contained junctions not only on their surface, but throughout the volume of the material?

The concept of creating substrates with a "volumetric" character is not new. For example, it has been known for some time that substrates with a distribution of junctions perpendicular to the plane of the wafer would deliver higher efficiency solar cells than substrates with only a surface planar junction. Problems with planar junctions arise from silicon's weak absorption of light in the near infrared. In the near infrared, electron-hole pairs are generated which may be several hundred microns from the junction at the surface of the silicon substrate. Thus, electrons must diffuse, or travel, a significant distance to the junction and many are lost due to recombination with holes prior to reaching the junction. By contrast, in volumetric substrates, with junctions distributed throughout the volume of the material, there always will be a junction nearby to collect and separate the electron-hole pairs.

In solar cell/photodiode applications, there have been two traditional approaches for generating substrates with active, non-planar junctions. One approach uses a conventional silicon wafer which has a very dense series of deep troughs etched into the silicon surface [1] prior to forming a p-n junction. This approach produced improved response in the near infrared, but is expensive and cannot be readily applied to other devices.

The second approach uses a composite of two interwoven semiconductor phases, one doped with p-type and the other with n-type elements. The process only can be applied to the limited set of semiconductors for which the two phases form a eutectic. A eutectic describes two components that are immiscible in the solid form and completely miscible in liquid form. Only two photodetectors have been processed using this composite approach and neither efficiently converted light into electricity at any wavelength [2].

Despite the disappointing results of these first eutectic devices, the composite approach seemed to be the most promising of the two and is the approach pursued by GTE. The basic concept of forming devices from multi-component materials with grown-in junctions is sound. Eutectic devices would break new ground in materials technology and have many potential applications in addition to photodetection. Previous difficulties arose due to the inherent limitations of the eutectic systems chosen.

In the first case, the carrier concentration of each component of the composite material could not be independently controlled or tailored to specific device needs. This was because the concentration of carriers in each component was determined by the mutual solubilities of the phases. A similar mutual doping of the phases occurred in the second system. Additional difficulties resulted from the lamellar distribution of phases. This microstructure complicated the analysis of the transport properties of each phase and frustrated efforts to form separate contacts to each semiconductor.

A FRESH APPROACH

GTE Laboratories' approach avoids many of these problems by using a rod-like, semiconductor-metal eutectic (SME) structure [3]. The SME composite incorporates Schottky rather than p-n junctions and the metallic phase appears in the form of rods. More than one million rods per square centimeter extend through the surface of each typical wafer. Since electrons are transported only within the semiconductor material, this geometry makes it possible to measure such properties as carrier concentration and Schottky barrier height. In addition, as long as high-purity metals are available, the carrier concentration of the semiconductor is controllable by using appropriate dopants.

GTE's approach represents a major departure from current electronic materials practices. Never before have two such dissimilar materials been used to create a material of electronic quality. In the past, conventional wisdom dictated that defects resulting from thermal expansion and lattice mismatch differences of the components would preclude their operation in electronic devices.

SUBSTRATE GROWTH MIRRORS SILICON PROCESS

The primary SME system examined by GTE is the silicon/tantalum disilicide eutectic. This system is particularly attractive because the boules, the cylinder shaped masses from which wafers are sliced and polished, can be grown in much the same manner as silicon crystals. Growth of a silicon boule begins by melting chunks of silicon in a quartz crucible. A single crystal of silicon is lowered onto the surface of the molten silicon and slowly pulled out to solidify the melt onto the single silicon crystal.

Adding tantalum (equal to 5.5 percent of the weight of the silicon) to the mixture and reproducing the crystal pulling process, produces a composite boule with a high density of tantalum disilicide rods in a single crystal silicon matrix.

Only minor adjustments need to be made between the two processes. The solidification temperature for the composite, called the eutectic temperature, is about 10 degrees Celcius below the melting point of silicon. Also, to avoid degeneration of the metallic rod structure into an irregular structure, the melt must be solidified at a temperature gradient exceeding a predetermined critical value.

Although the process is mechanically similar to standard silicon crystal growth, the atomic motion at the solid-liquid interface is very different. During the growth of a single type material, like silicon, the composition of the melt at the solid-liquid interface is laterally uniform. Differences in the solubility of certain impurities in the solid versus the liquid create small compositional gradients at the interface along the growth direction, but not in the growth plane.

During eutectic growth, however, nucleation of the solid tantalum disilicide lowers the concentration of tantalum in the melt. Similarly, nucleation of solid silicon adjacent to the tantalum discilicide causes rejection of excess tantalum in the melt. Thus, during eutectic growth, a diffusion couple is created in the plane of the solid-liquid interface. This diffusion process ties the spacing of the rods to the growth rate of the material.

In all rod-like eutectics, the interrod spacing is inversely proportional to the square root of the growth rate. Therefore, the higher the growth rate, the smaller the interrod spacing and the higher the density of rods. A growth rate typical for silicon (5 centimeters per hour) yields an interrod spacing of about 16 micrometers. By simply applying a growth rate of 20 centimeters per hour, a rod spacing of 8 micrometers, which is suitable for electronic devices, can be produced [4].

A typical microstructure of a silicon-tantalum disilicide composite grown at 20 centimeters

per hour is illustrated in Figure 1. The rods are 1 micrometer in diameter and constitute 2 percent of the volume of the composite. Unlike most electronic materials where lithographic techniques are used to space junctions, the natural process of eutectic growth does not produce a material with lattice-like distribution of junctions. Instead, the turbulent melt flow and the crystallographic dependence of the surface energies on the composite materials produce some misalignment of the rods and a structure which is neither regular nor completely random.

Doping of the semiconductor matrix is accomplished by using doped silicon as a charge and by adding n-type and p-type elements to the melt in cases where high doping levels are desired. The effectiveness of the doping procedure is determined by measuring the resistivity and Hall coefficient of the composite samples in which the rods are oriented perpendicular to the axis of current flow. Using this approach, both n-type and p-type composites have been obtained with carrier concentrations between 10^{15} cm^{3} and 10^{18} cm^{3}.

These transport measurements reveal several important characteristics about the composites. First, the mobility of the carriers in any given concentration is characteristic of single crystal silicon and the carrier mobility is not degraded by the metallic rods.

Figure 1. A scanning electron micrograph showing the two phase microstructure of a silicon/tantalum disilicide composite. The white areas represent the tantalum disilicide rods. The dark background is the silicon matrix.

Secondly, the segregation of the p-type and n-type dopants along the length of the boules also is characteristic of single crystal silicon growth. For example, tantalum in the melt does not significantly alter the partitioning of the composite between its solid and liquid phases. Finally, the minimum carrier concentrations observed (10^{15} cm^{3}) is suitable for the fabrication of many devices that would utilize Schottky junctions.

Not surprisingly, defect densities in the silicon matrix have been found to be high. Examination of the material through electron microscopy and x-ray diffraction indicates that the silicon matrix contains between 10^{6} and 10^{7} lattice dislocations per square centimeter. These defects are a result of stresses caused by the thermal expansion mismatch of the silicon and tantalum disilicide phases.

SUBSTRATE CHARACTERISTICS EXAMINED

At the junction of any two materials, the electron free energy, called the Fermi energy, must remain constant. Any change in the Fermi energy causes a net movement of carriers until an equilibrium is achieved. Establishing this electron equilibrium between a metal and a semiconductor results in the Schottky barrier. Due to the initial displacement of carriers in the semiconductor upon the joining of the two phases, a region in the semiconductor extending outward from the potential barrier at the metal/semiconductor interface is depleted from carriers. This region, called the depletion zone, is characteristic of any Schottky junction and contains a built-in electric field that keeps free carriers out of the region.

It is already well known that a polycrystalline film of tantalum disilicide on silicon yields a Schottky barrier of 0.6 electron volts (eV). GTE scientists did not know, however, if a junction formed in a silicon-tantalum disilicide eutectic would exhibit the same characteristics. Consequently, GTE researchers sought to characterize the interface as fully as possible.

Three techniques commonly used to examine planar junctions were employed. The techniques used were current-voltage, capacitance-voltage, and electron- beam-induced current (EBIC). Together, these examination techniques demonstrated that the perpendicular junctions are very similar to more conventionally formed thin-film junctions.

Fabrication of test devices required the development of methods for creating Schottky contacts for connecting the rods and for obtaining an ohmic contact. An ohmic contact was produced as it is in silicon devices by forming a metallic film on top of a heavily doped surface layer of silicon. This was accomplished using an Au-Sb film.

The contact to the rods had to be made without forming an ohmic contact to the silicon matrix between the rods. A metallic film could be used if it formed a Schottky contact to the silicon matrix with a barrier exceeding the barrier height of the silicon-tantalum disilicide interface and if it had a relatively small junction area. A metallic film of cobalt disilicide with a Schottky barrier of 0.64 eV, lithographically patterned on the composite surface to cover a known number of rods, was used. For the 500 micrometer thick wafer, a silicon-cobalt disilicide junction area was just three percent of the silicon-tantalum disilicide junction area. The fabrication technique employed is schematically shown in Figure 2 (page 8).

Using this contact procedure with a 125 micrometer diameter cobalt disilicide surface contact, the voltage necessary to force a given current of electrons across the junction was measured. When electrons are directed from the silicon to the silicide, the forward voltage reduces the barrier and current readily flows. When electron flow is from the silicide to the silicon, currents remain small since the barrier that electrons must overcome is fixed and independent of the reverse voltage. For this reason, the current is a reflection of the ability of electrons to be activated over the built-in Schottky barrier. The magnitude of the current within this limit indicates that the tantalum disilicide-silicon junction has a Schottky barrier height of 0.62 eV, a value very close to the planar, thin-film value [5].

Due to the separation of charge upon formation of the junction, the interface also has a capacitance associated with it. This capacitance, dependent on the depletion zone width or charge separation, is an important factor in determining the speed of devices. A planar junction, modeled after a parallel plate capacitor, has a capacitance which decreases inversely with the depletion zone width. This simple relationship was not obtained in the composite diode. As a result of the rod-like geometry of the junctions, the capacitance behaves like a coaxial capacitor, decreasing more slowly with applied bias than it would for a planar junction.

The Electron-Beam-Induced Current (EBIC) technique, also used to characterize the junctions, actually enabled imaging the depletion zones [6]. In this technique, the plane of the wafer opposite the surface cobalt disilicide is scanned with a scanning electron microscope (SEM). As the electron beam is scanned, electrons and holes are generated in the silicon. Electrons and holes that are separated prior to recombination by the electric field associated with the junctions contribute a short-circuit current, just as with photogenerated electron-hole pairs. By synchronizing the short-circuit current with the position of the scanning beam, an image of the composite is formed in which contrast is determined by the charge-collection efficiency.

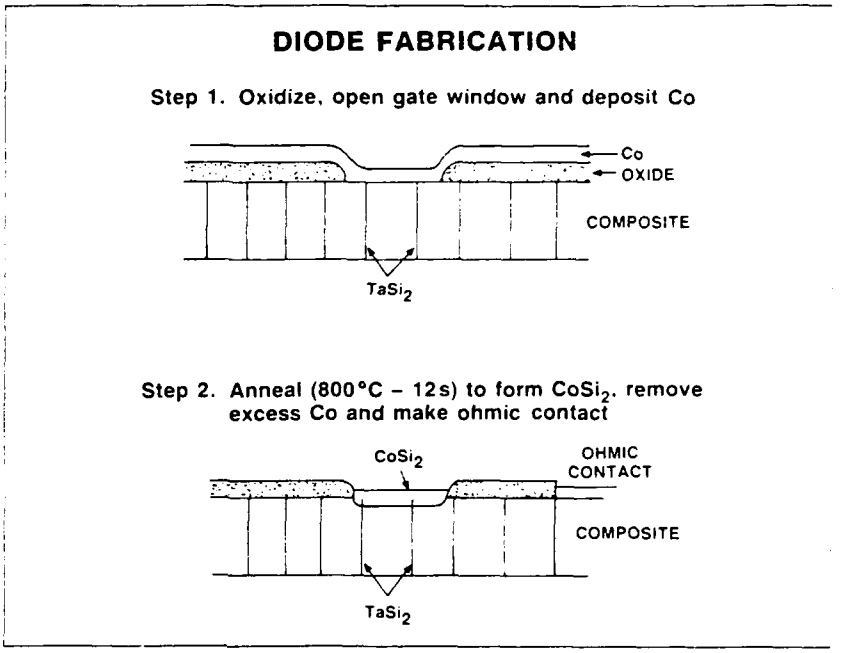


Figure 2. A schematic showing the processing steps required to form the gate contact to the junctions.

Thus, in the composite diode, the short-circuit current will be zero when the electron beam is on the tantalum disilicide rod and the image appears dark. When the beam is incident on the silicon included in the depletion zone, the charge-collection efficiency is at its highest and the EBIC image appears the brightest. This is because the built-in electric field effectively separates electron-hole pairs. Less current is collected when the beam is incident on silicon outside the depletion zone since some recombination occurs before the electrons and holes diffuse to the junction.

A secondary electron image of a small area containing five rods and a EBIC image of the same area when the diode is unbiased and biased at five volts is

illustrated in Figure 3. Around each rod, a bright halo, indicating the depletion zone, is observed. Biasing the rods causes the depletion zones to expand and interpenetrate.

LIGHT-DETECTING ABILITIES DEMONSTRATED

Since the depletion zones are the active regions of any device processed using this eutectic composite substrate, the ability to image them in the EBIC mode is important. EBIC, in conjunction with other characterization techniques, demonstrate that the substrates are truly "volumetric." EBIC also demonstrates that the composite substrate could also act as a photodetector with an inherent spatial resolution limited only by the spacing of the rods.

The efficiency of any photodiode is its most critical feature. As previously discussed, the wavelength dependence of the absorption of light in a silicon photodiode makes it advantageous to have a volumetric distribution of junctions to separate the electron-hole pairs. In a silicon-tantalum disilicide rod-like eutectic photodiode, independent of wavelength between the far ultraviolet (400 nanometers or 400 nm) and the near infrared (1000 nm), the distance that electrons or holes must diffuse to be collected is fixed at approximately half the interrod spacing. Therefore, the quantum efficiency (i.e., the fraction of electrons collected per incident photon) should be independent of wavelength. This characteristic was in fact observed during GTE research demonstrations.

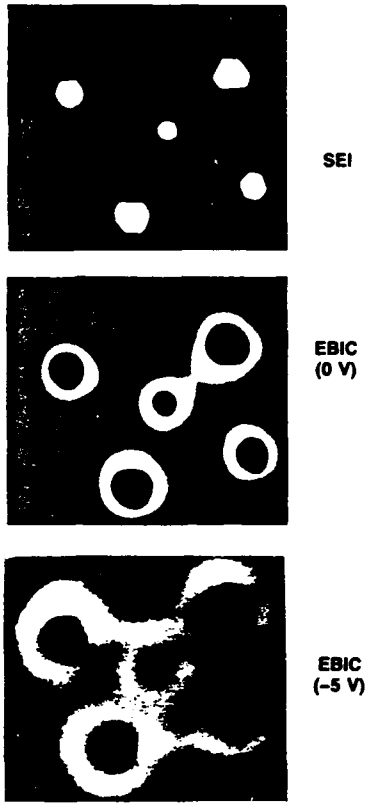


Figure 3. Scanning electron micrographs of a portion of the Si-$TaSi_2$ eutectic diode. a) An image of 5 $TaSi_2$ rods in a Si matrix. b) The corresponding EBIC image for the gate without a bias voltage to the rods. The bright halos around the rods outline the depletion zones. c) EBIC image at reverse bias voltage of 5V. The bias voltage expands the depletion zones.

During GTE's research, unbiased photodiodes (shown in Figure 4) yielded a quantum efficiency of approximately 50 percent throughout the wavelength range. Biasing the photodiodes further improves efficiency by expanding the device's depletion zone. Compared to conventional planar junction photodiodes, the eutectic diodes display a constant quantum efficiency over a much wider range and perform much more efficiently in the near infrared light range [7].

Although performance of these active substrates already is quite good, improvements can be expected by reducing the number of defects and hence the number of electron-hole recombination centers located in the silicon matrix and/or by enlarging the depletion zones.

GROWING TRANSISTORS

As previously discussed, the depletion zones surrounding the tantalum disilicide rods in the composite can be expanded with a bias voltage. Because the silicon regions between the rods represent a conductive channel, use of a voltage to narrow or completely close-off this channel creates a voltage-controlled resistor. Such a resistor represents the operational definition of a field effect transistor (FET).

These transistors were processed using the same, simple

contact procedure which was developed for diodes and differs from the processing of conventional transistors in that junctions do not need to be formed. The junctions are already present in the substrate just waiting to be tapped.

A simple concentric ring design was employed to demonstrate such a transistor. Ohmic contacts, which employ the Au-Sb films, are located on a small dot at the center of the ring and on an outer ring which circles the dot. These, respectively, provide the transistor's source and drain contacts. Another ring located between the source and drain forms the gate, which was contacted using a cobalt disilicide film. The gate provides voltage control for the device. Current flows from the source, through the silicon channels between the rods, under the gate contact and toward the drain.

Expansion of the depletion zones around the rods under the gate contact increases the source-to-drain channel resistance. When the bias voltage is sufficient to cause the depletion zones from adjacent rods to overlap, the channel is "pinched-off." Thus, the built-in electric field blocks current flow and the device is in its "off-state."

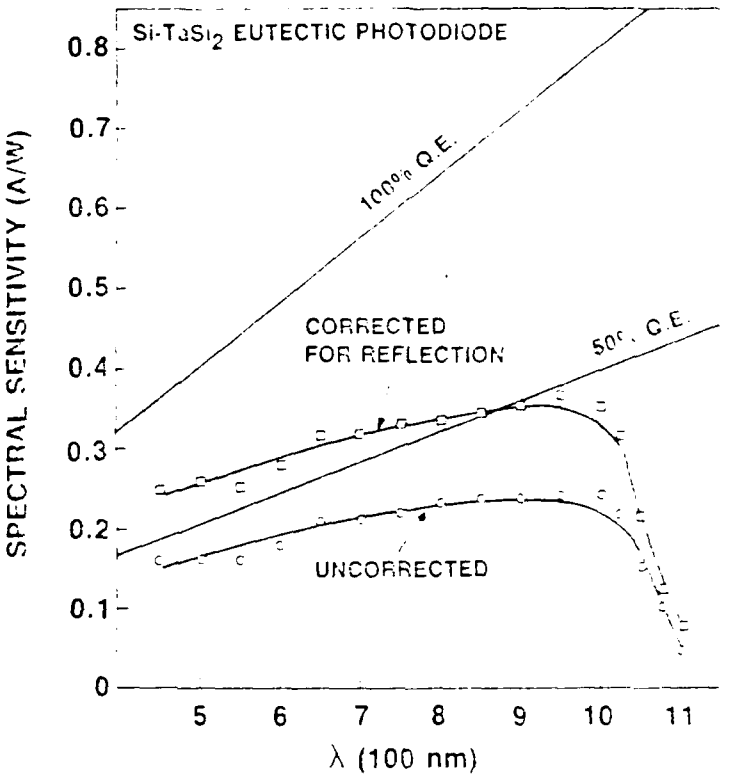


Figure 4. The spectral sensitivity of a eutectic photodiode. The raw data (uncorrected) is also shown after correction for reflection losses. The quantum efficiency of the detector is approximately constant between 450 nm and 1000 nm due to the invariance of the distance between electron-hole pair generation and collection.

Fabrication of such transistors benefit from the advantage of both simplicity and three-dimensionality. The devices are simpler to process than conventional devices because the gate structure is already built into the material. This makes traditional processing steps, such as epitaxial growth, diffusion and/or implantation, unnecessary. Another step, fine-line lithography, also is unnecessary because the spacing of the gates is determined by the growth rate of the boule. In addition, the metallic rods extending through the wafer give the device a distinctly nonplanar design that will be useful in designing high-power devices.

As illustrated in Figure 5, the characteristics displayed by the first transistors processed are remarkably good and are very similar to the characteristics of a junction field effect transistor (JFET). The output of the transistor is determined by the maximum current (30 mA) and maximum voltage (330 V). This translates into an output power of 9 watts, which is in the operating realm of power transistors.

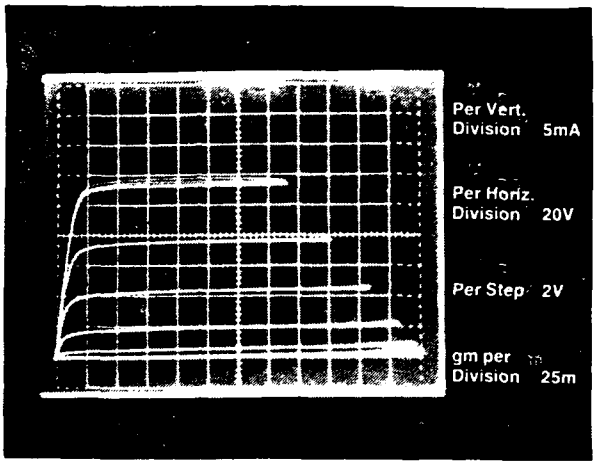


Figure 5. The transistor characteristics of a typical eutectic composite transistor.

The potential for SME devices to switch high power will depend on a number of factors, the most important factor being the breakdown voltage. The maximum source-to-drain voltage of any solid state device is limited by the voltage that induces avalanche breakdown. The device must always be operated below this voltage. Avalanche breakdown results when free carriers activated over the Schottky barrier are accelerated into the semiconductor by an electric field sufficient to cause impact ionization of electrons and holes. When this happens, the device resistance becomes small and it cannot support additional voltage.

Interestingly, SME materials appear to be unusually resistant to this type of breakdown. For example, avalanche breakdown in a conventional device with an electron carrier concentration equal to the device illustrated in Figure 5 would limit maximum operating voltage to 200 V. The eutectic device enables this limit to be exceeded by 100 V. GTE researchers hypothesize that the built-in electric field associated with junctions that neighbor the gate may 'soften' the electric field at the biased junction, thereby extending the maximum device voltage. Optimization of this affect could yield very high voltage devices [8].

A SPRINGBOARD FOR FUTURE RESEARCH

Device applications presented in this article for active substrates represent only the beginning of possible uses for such materials. As the science and technology of these new materials and devices develop, many new, versatile applications will emerge. The first demonstration by GTE scientists that two-phase, equilibrium semiconductor-based alloys can be fabricated simply into useful electronic devices serves as a springboard for the development of other novel devices and new research areas.

Initial applications likely will begin with the basic silicon-tantalum disilicide eutectic substrate as the building block and include large-area, near infared photodectors or simple voltage controlled resistors and current limiting devices. Further development of the material will unfold more sophisticated applications. For example, reduction of the silicon matrix carrier concentration could expand applications of SME devices as high-voltage transistors.

In addition, the ability to deposit epitaxial layers of silicon or other semiconductors onto the material could create tandem devices that would benefit from the properties of both the SME substrate and the surface semiconductor layer. For example, the output of photodiode arrays in the eutectic composite could be directed into a conventional epitaxial film to form high resolution, low crosstalk arrays at wavelengths of approximately one micrometer. Conventional silicon devices suffer from extensive crosstalk between pixels at these wavelengths. Work on such tandem concepts is currently being pursued by GTE researchers.

The development of similar SME composites based on germanium or gallium arsenide would open up additional possibilities. For example, germanium-based SME photodetectors would result in high-speed, high quantum efficiency detectors at 1.3 and 1.55 micrometers, the wavelengths of importance for optical communication systems. Gallium arsenide-based eutectic composites would further extend the high power, high frequency characteristics of SME transistors.

In a broader sense, these developments may change the direction of semiconductor research to include equilibrium semiconductor alloy structures. Previous tenets of semiconductor science disregarded equilibrium microstructures because of fears that high defect densities or unacceptable impurity levels would result. GTE's work suggests, however, that the fears

concerning impurities are unfounded. Further, the beneficial effects of the eutectic microstructure may override any disadvantages. The eutectic photodiode, for example, yields high quantum efficiencies by compensating for the defect-reduced carrier lifetime with closely spaced junctions that reduce the need for long diffusion distances. Thus, the same features that create a potential problem also create a solution.

In summary, silicon-based substrates with active grown-in junctions have been used to fabricate novel photodiodes and transistors. The work signifies the emergence of a new class of materials that can act as active electronic substrates. The number of new materials in this class is large. The eutectic phase diagram is perhaps the most common of all and alone provides more than 10 systems between silicon and silicides which may be explored. Many additional gallium arsenide-based semiconductor-metal eutectics remain to be discovered and developed. Full research into these electronic composite materials will require a significant effort. GTE researchers believe, however, that the momentum for further research exists and that the rewards will be great.

ACKNOWLEDGEMENTS

This work was supported in part by the Air Force Office of Scientific Research under contract F49620-86C-0034 and by the SDIO/IST, managed by the office of Naval Research under contract N00014-86C-0595.

REFERENCES

1.) R.I. Frank, J.L. Goodrich and R. Kaplow, "A low series resistance silicon photovoltaic cell for high intensity applications", **Conf. Rec. 14th IEEE Photovoltaic Spec. Conf., IEEE**, p. 1350 (1980).

2.) L.A.H. van Hoof and W. Albers, "Eutectic heterostructure in the Cdte-Gate system", **J.Appl.Phys., 52,** p. 3476, (1981).

3.) B.M. Ditchek, "Bridgman and Czochralski Growth of Ge-$TiGe_2$ Eutectic Composites", **J. Crystal Growth,** 75, p. 264 (1986).

4.) B.M. Ditchek, B.G. Yacobi and M. Levinson, "Depletion zone limited transport in Si-$TaSi_2$ eutectic composites, **J. Appl. Phys.,** to be published March 1, 1988.

5.) B.M. Ditchek and M. Levinson, "Si-$TaSi_2$ *in situ* eutectic composite diodes", **Appl. Phys. Lett.,** 49, p. 1656 (1986).

6.) B.G. Yacobi and B.M. Ditchek, "Characterization of multiple *in situ* junctions in Si-$TaSi_2$ composites by charge-collection microscopy", **Appl. Phys. Lett.,** 50, p. 1083, (1987).

7.) B.M. Ditchek, B.G. Yacobi and M. Levinson, "Novel high quantum efficiency Si-$TaSi_2$ eutectic photodiodes," **Appl. Phys. Lett.,** 51, p. 267 (1987).

8.) B.M. Ditchek, T.R. Middleton, P.G. Rossoni and B.G. Yacobi, "A novel high voltage transistor fabricated using the *in situ* junctions in a Si-$SiTa_2$ eutectic composite", submitted to **Appl. Phys. Lett.**

Appendix F

Semiconductor-Metal Eutectic Composites for High-Power Switching

Semiconductor-metal eutectic composites for high-power switching

B.M. Ditchek and B.G. Yacobi

GTE Laboratories Incorporated
40 Sylvan Road, Waltham, MA 02254

ABSTRACT

A novel electronic material, a Si-$TaSi_2$ semiconductor-metal eutectic composite, offers promise in high-power switching applications. In this paper, the basic electronic properties of the material are briefly described. It is shown that the *in situ* Schottky junctions inherent to the material can be used to fabricate transistors. The advantages of these devices are their volumetric current transport and their unusual resistance to avalanche breakdown.

1. INTRODUCTION

Pulsed power conditioning for space-based energy systems requires switches that handle currents in excess of 1 kA and block voltages greater than 50 kV. The most attractive switches capable of meeting these requirements are either of the gaseous or solid-state type. The solid-state switches are generally of the photoconductive type, in which a high-resistivity (about 1000 Ω-cm) slab of Si is illuminated with a pulsed laser with a wavelength near 1 μm. In this approach, the laser pulse turns the switch on.[1] Difficulties with this switch result from high leakage currents in the "off-state" and premature surface breakdown. A completely solid-state transistor-like switch would be an attractive alternative to the photoconductive switch because it would eliminate the need for a high-power laser. However, transistors based on conventional semiconductor materials that can block such large voltages and handle such large currents are not readily available.

The main obstacle to engineering devices to block voltages in excess of 1 kV is avalanche breakdown.[2] Avalanche breakdown occurs when carriers overcoming the barrier at the gate gain sufficient energy when accelerated by the large electric field in the depletion zone to cause multiple ionization of bound charge carriers.

The maximum breakdown voltage is determined by the carrier concentration in the semiconductor. For example, a carrier concentration less than 2.5×10^{14} cm^{-3} is needed for a Si device to block 1000 V.[2] Higher blocking voltages can only be attained by lowering the carrier concentration, which has the adverse effect of lowering the current-handling ability of the device in the "on-state." In practice, for a given carrier concentration, breakdown tends to occur at a lower voltage than in the example above because of field concentration at the gate edges. Although many improvements in FET design and performance have occurred in recent years, the basic limitations imposed by the carrier concentration-avalanche breakdown voltage relationship have restricted the development of transistors for pulsed-power operation. This is true independent of whether the semiconductor material is Si or GaAs.

Because of the inherent limitations of conventional devices, substantial improvements in the power-handling capabilities of solid-state switches will require a radically different approach. Recently, the development of a new class of electronic materials, semiconductor-metal eutectic composites, for high-power switching applications has been undertaken.[3-6] Like a bulk semiconductor, this material can be applied to high-power switching using the photoconductive approach or as gate-voltage controlled transistors. The main focus of the work to date has been to demonstrate transistor action in this material and to evaluate its applicability to pulsed-power-type switching.

Semiconductor-metal eutectic composite materials are composed of a high density (of the order of 10^6 rods/cm^2) of aligned metallic rods in a semiconducting matrix. A Schottky rectifying junction is present at the interface between each of the metallic rods and the semiconducting matrix. These materials are radically different from conventional semiconductor wafers in several ways: 1) the junctions are distributed throughout the entire volume of the wafer, thereby enabling the handling of high currents; 2) the junctions are formed *in situ* upon solidification from the melt and do not have to be lithographically patterned on the wafer surface; and 3) the rod or junction density is determined by the solidification rate and generally exceeds 10^6 cm^{-2}. In this report, the growth, electronic properties and device physics for one of these materials, the Si-$TaSi_2$ system, are discussed. It is shown that high-voltage transistors made with these materials have a three-dimensional character and, most important for high-power switching applications, are resistant to avalanche breakdown.

2. GROWTH AND CHARACTERIZATION OF SME MATERIALS

2.1 Composite growth and microstructure

The composite materials are grown by conventional crystal growth techniques. For example, growth of the Si-$TaSi_2$ eutectic is similar to the growth of Si crystals. Crystals of both materials are grown by the Czochralski crystal pulling technique using a Si seed crystal. The difference is in the charge: the single crystal Si boule is pulled from a pure Si melt, while the Si-$TaSi_2$ quasi-single crystal is pulled from a melt containing both Si and Ta.[3,6] The composition of the melt is chosen such that it corresponds to the eutectic composition. At this composition the homogenous melt simultaneously solidifies into two distinct phases, Si and $TaSi_2$. The eutectic composition corresponds to 2 v/o $TaSi_2$. Minimization of interface energy results in the rod-like distribution of the minor phase, in this case $TaSi_2$.[7] The interrod spacing, λ, is related to the solidification rate, v, according to

$$\lambda = A\, v^{-1/2},$$

where A is a constant dependent on the diffusion coefficient in the liquid and the interfacial energy.[8] A schematic of the microstructure

of a rod-like semiconductor-metal eutectic is shown in Figure 1(a). Figure 1(b) shows the actual microstructure of a Si-$TaSi_2$ composite grown at a rate of 20 cm/h. For the Si-$TaSi_2$ system, $A = 6.0 \pm 0.8 \times 10^{-5}$ $cm^{-3/2}$ $s^{-1/2}$.[6] The entire composite is a quasi-single crystal with a (111)-oriented Si matrix. Defects in the Si matrix, due to the thermal expansion mismatch stresses between the Si and the $TaSi_2$, tend to be high, of the order of 10^6–10^7 dislocations/cm^2.[9]

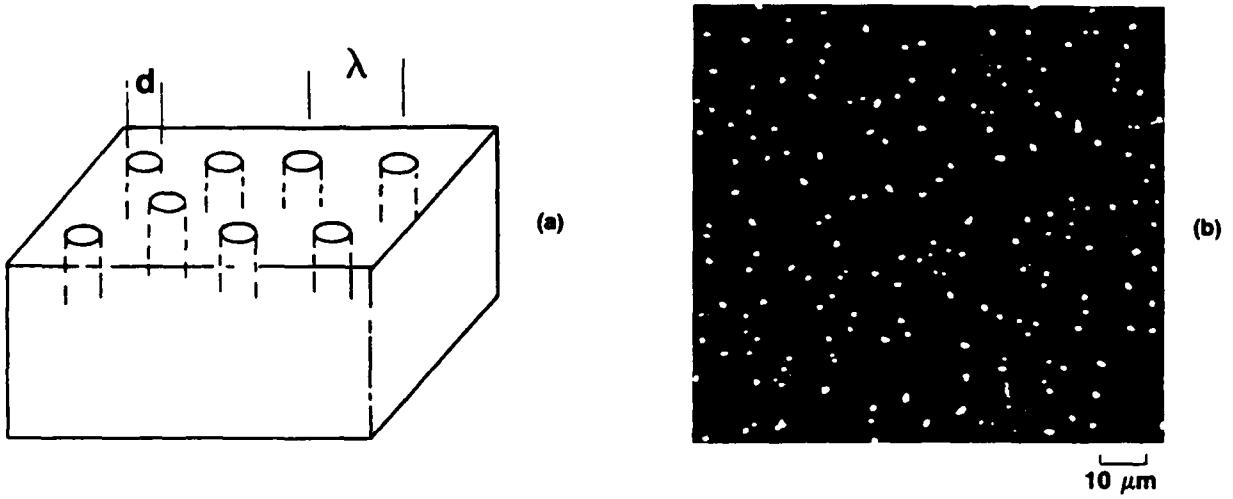


Figure 1. (a) A schematic of the microstructure of a semiconductor-metal eutectic composite. (b) The actual microstructure showing the rod-like distribution of the Si-$TaSi_2$ eutectic composite grown at 20 cm/h.

2.2 Electronic properties

Semiconductor-metal eutectic composites are composed of a high density of cylindrical Schottky junctions. These junctions enable control of the current flow using a bias voltage, and they also affect the resistance to current flow even without a bias voltage. The *in situ* junctions have been characterized by current-voltage, capacitance-voltage, electron-beam-induced current (EBIC) and deep-level transient spectroscopy techniques. All of these techniques require the availability of low-leakage diodes. These diodes were fabricated in wafers having Si matrix carrier concentrations of the order of 10^{15} cm^{-3} by forming on the wafer surface a metallic film that provided an ohmic contact to the $TaSi_2$ rods and a Schottky contact to the Si matrix material between the rods. This film, composed of $CoSi_2$, acts as the contact to the junctions. An evaporated and annealed Au-Sb ohmic contact was formed at a position away from the active rods contacted by the silicide surface film. This technique provided nearly ideal diodes.[3] I-V analysis indicated that the Si/$TaSi_2$ junction was characterized by a Schottky barrier height of 0.62 eV.[3] The capacitance of the junction was commensurate with the cylindrical geometry of the junction, the carrier concentration and the junction area.

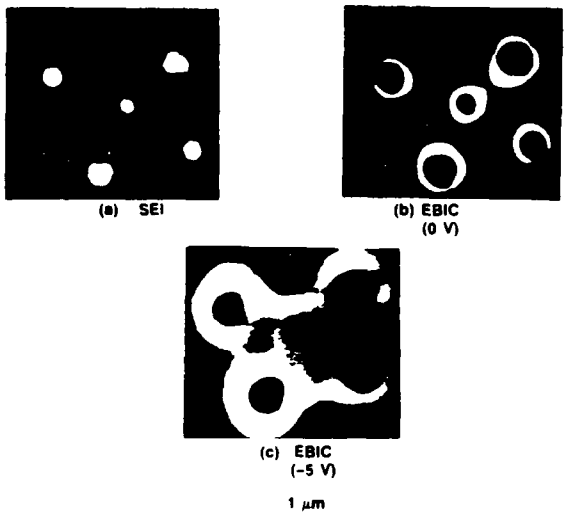


Figure 2. Scanning electron micrographs of the portion of the Si-$TaSi_2$ eutectic diode. (a) Secondary electron image of $TaSi_2$ rods embedded in a Si matrix. (b) Corresponding EBIC image (unbiased). (c) EBIC image at a reverse bias of 5 V.

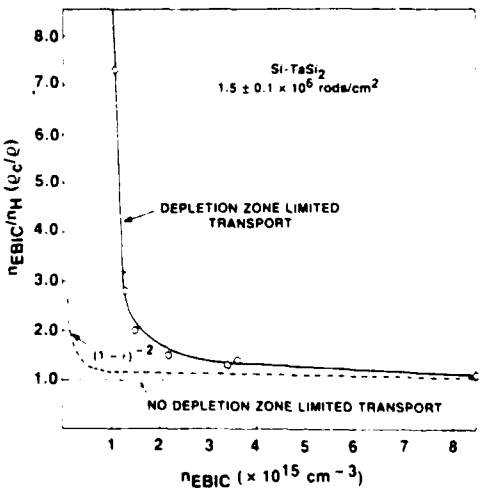


Figure 3. The increase in the resistivity of the composite relative to the resistivity of the Si matrix material as a function of the actual carrier concentration in the Si matrix measured using the EBIC technique. The significant increase in composite resistivity below a carrier concentration of about 2×10^{15} cm^{-3} is due to depletion zone limited transport.

A reverse bias applied to the junction reduced the capacitance due to expansion of the depletion zone. The expansion of the depletion zone around the rods was graphically demonstrated using the EBIC technique.[4] Figure 2 shows a set of rods imaged in the scanning electron microscope using a) secondary electron imaging, b) the EBIC mode without a bias voltage, and c) the EBIC mode with a reverse bias voltage of −5 V. The depletion zone is indicated by the bright halo around the rods in the EBIC images. The increased diameter of the halo with the reverse bias indicates expansion of the depletion zone. These results are important in a number of ways. First, they demonstrate that the application of a bias voltage to the silicide rods causes an expansion of the depletion zones to the point of overlap. Overlap of depletion zones, corresponding to "pinch-off" in a three-terminal transistor, represents the transformation of the material from a semiconducting to an insulating state. Second, by comparing the size of the depletion zone as a function of bias voltage with that predicted by theory for a cylindrical junction, the carrier concentration of the Si matrix may be accurately determined.[6] Finally, by comparing these carrier concentration measurements with Hall effect carrier concentration measurements, it is possible to determine the effect of depletion zones on the composite resistivity.[6]

Clearly, as the volume fraction of the composite consumed by the depletion zones increases, the resistivity of the composite material compared to the resistivity of the undepleted Si material between the rods also increases. Figure 3 shows the ratio of composite resistivity to the Si resistivity, ϱ_c/ϱ, as a function of the Si matrix carrier concentration for the case of a rod density of $1.5 \pm 0.1 \times 10^6$ rods/cm^2.[6] The resistivity of the composite is increased when the carrier concentration drops below 2×10^{15} cm^{-3} or when the depletion zone volume fraction exceeds about 7%. The resistance increase is due both to loss of carriers and current streamlining around the rods.[6]

3. TRANSISTORS

Because wafers of the SME composite material contain *in situ* junctions, fabrication of transistors simply requires formation of three surface contacts for the source, drain, and gate. Using wafers cut transverse to the growth direction so that the rods were normal to the plane of the wafers, contacts were lithographically patterned in a concentric ring design. Figure 4 shows a quarter section of the ring pattern, and Figure 5 shows several wafers patterned with devices.

To fabricate the device, the wafers were thermally oxidized at 1000 °C to grow a 0.3-μm-thick oxide. Vias in the oxide were opened for the surface contacts. The central gate contact ring, similar to the diode contact, was a 0.2-μm-thick $CoSi_2$ film. The source and drain contacts were annealed Au-Sb films. In certain cases, $CoSi_2$/n$^+$ contacts were used for the source and drain.

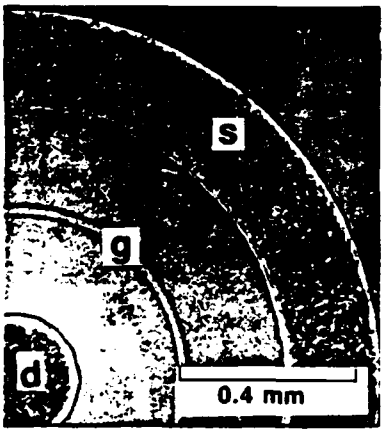


Figure 4. A quarter section of the concentric ring pattern of source, gate, and drain contacts used to fabricate the transistor.

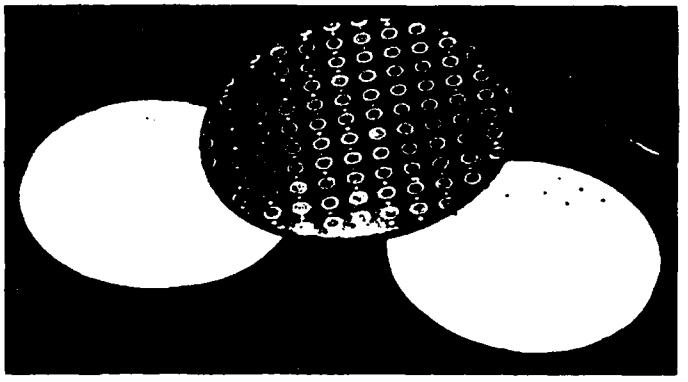


Figure 5. Several eutectic composite wafers with arrays of discrete transistors.

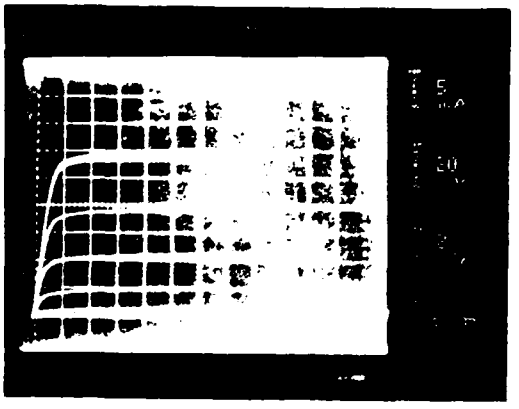
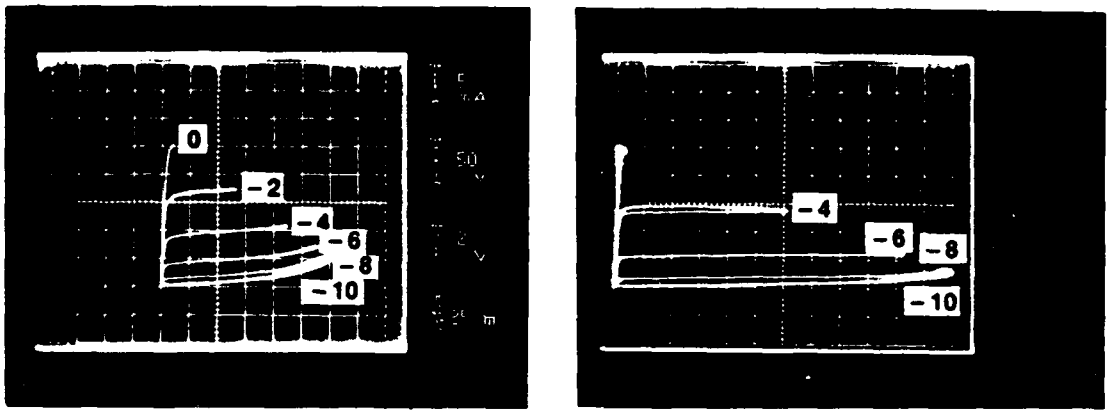


Figure 6. Typical characteristics of a eutectic composite transistor.



(a) (b)

Figure 7. The characteristics of a eutectic composite device tested with a wafer thickness of (a) 250 μm, and (b) after thinning to a wafer thickness of 125 μm.

An example of the current-voltage characteristics of a eutectic composite transistor with the drain current plotted against the drain voltages for different gate voltage is shown in Figure 6. The carrier concentration of the Si matrix is 2×10^{15} cm^{-3}, and the resistivity of the composite along the direction perpendicular to the rod axis is 20 Ω-cm. The substrate is 250 μm thick and has the surface contact dimensions shown in Figure 4. The basic characteristics of the device are similar to those of a conventional metal-semiconductor field effect transistor (MESFET) in that they display a linear region at drain voltages less than the "pinch-off" voltage and a saturation region when the drain voltage exceeds the "pinch-off" voltage. For this device the "pinch-off" voltage is -10 V.

The device shown in Figure 6 readily blocks a drain voltage of 240 V; avalanche breakdown is expected at 190 V for this carrier concentration. Thus the microstructure of the eutectic device delays avalanche breakdown beyond the value expected for a guarded planar device. The device ultimately failed just above 325 V. Failure was not by avalanche breakdown but by a mechanism that destroyed the device characteristics. Unlike avalanche breakdown, this mechanism is not an inherent materials limitation but depends on such parameters as the spacing between the gate and drain contacts and the thickness of the wafer.

To examine the effect of thickness on device performance, a 500-μm-thick wafer with a device that failed prematurely at 45 V was thinned to 250 μm and retested. The wafer had a Si matrix carrier concentration of 3×10^{15} cm^{-3}. Thinning the wafer resulted in recovery of the same device and yielded the characteristics displayed in Figure 7(a). The device characteristics show a drain voltage of 300 V at a gate voltage of -10 V. Some leakage is observed at the high drain voltages. The unbiased curve is cut off at low voltages because a high series resistor was used in the curve tracer to minimize heating effects. The device failed catastrophically at a drain voltage of 325 V. The wafer was thinned further to 125 μm, and the device was retested. The characteristics of the same device in the thinner wafer are shown in Figure 7(b). Again, the device recoved and operated with a drain voltage of 600 V. This value is at least three times the blocking voltage of a conventional planar device in a wafer of the same carrier concentration. The high-current portion of these characteristics is similarly cut off to avoid heating effects. For this device the gate-to-drain contact separation is 135 μm. With a 600 V drop over this distance, the average field exceeds 4×10^4 V/cm.

These experiments reveal two key features of these devices. Most importantly, the experiments demonstrated that SME materials are usually resistant to avalanche breakdown. To our knowledge, the critical voltage for avalanche breakdown has never been exceeded with conventional devices. Thus, for the first eutectic devices to exceed the threshold for avalanche breakdown by a factor of 3 is very promising. In addition, it was found that the saturation current (for the unbiased case) was approximately proportional to the wafer thickness, verifying that the current channel of the eutectic device occupies the wafer thickness.

The mechanism whereby avalanche breakdown is delayed and the actual mechanism causing device failure have yet to be determined. The resistance to avalanche breakdown is probably related to the presence of cylindrical junctions between the gate and drain. This is the primary difference between these devices and conventional devices. It is suggested that the depletion zones around these floating rods interact with the depletion zone extending outward from the gate rods with the net effect of reducing the maximum electric field. A reduction in the field for a given carrier concentration is required to explain this effect. Numerical modeling studies are under way to test this hypothesis.

The actual voltage limiting device operation has been found to depend on wafer thickness and the spacing between gate and drain contacts. These two variables are related. Because the rods tend to diverge (EBIC measurements indicate a maximum divergence angle of 6°),[4] the $TaSi_2$ extension of the gate and drain contacts are more closely spaced on the back side of the wafer than on the side with the surface contacts. It is therefore likely that failure is related to punch-through of the gate depletion zone to the drain contact. Thinning the wafer has the effect of increasing the back surface spacing between gate and drain, thereby increasing the drain voltage necessary to expand the depletion zone to the point of punch-through. If this is applicable, the drain voltage of devices can be increased without thinning the wafer (and therefore losing current density) by increasing the gate to drain distance at the expense of the source-to-gate distance.

4. DISCUSSION

The Si-$TaSi_2$ system, a semiconductor-metal eutectic composite material, is representative of a new class of electronic materials that appears to hold great promise in solid-state pulsed-power switching. Due to the unique geometry of grown-in cylindrical junctions that are oriented perpendicular to the wafer surface, eutectic composite transistors are not subject to the same limitations as conventional planar junction transistors. The volumetric nature of these new devices enables the handling of increasing current density (per unit wafer surface area) with an increase of the wafer thickness. Furthermore, the material's inherent resistance to avalanche breakdown may enable significant improvements in the maximum blocking voltage that is possible with solid-state transistor devices. Analysis of present device parameters indicates that blocking voltages exceeding 1000 V and current densities as high as 40 A/cm^2 can be expected. Additional optimization in the processing of this and other SME materials, along with better understanding of the mechanisms limiting avalanche breakdown, may lead to substantial improvements in their power switching capabilities.

5. ACKNOWLEDGMENTS

Assistance in the growth of the material and the fabrication of devices by Tom Middleton is gratefully acknowledged. Also device modeling studies by Phil Rossoni contributed to our understanding of device operation. This work was sponsored in part by the Air Force Office of Scientific Research under contract F49620-86-C-0034 and by the SDIO/IST and managed by the Office of Naval Research under contract N00014-86-C-0595.

REFERENCES

1. W.C. Nunnally and R.B. Hammand, *Appl. Phys. 44,* 980 (1984).
2. S.M. Sze, *Physics of Semiconductor Devices,* Wiley, New York (1969).
3. B.M. Ditchek and M. Levinson, *Appl. Phys. Lett. 49,* 1656 (1986).
4. B.G. Yacobi and B.M. Ditchek, *Appl. Phys. Lett. 50,* 1083 (1987).
5. M. Levinson, B.M. Ditchek, and B.G. Yacobi, *Appl. Phys. Lett. 50,* 1906 (1987).
6. B.M. Ditchek, B.G. Yacobi, and M. Levinson, to appear in *J. Appl. Phys.* (March 1988).
7. K.A. Jackson and J.D. Hunt, *Trans. Metall. Soc. AIME* 236, 1129 (1966).
8. F.R. Mollard and M.C. Flemings, *Trans. Metall. Soc. AIME* 239, 1526 (1967).
9. B.G. Yacobi and B.M. Ditchek, 5th Oxford Conf. on Microscopy of Semiconductor Materials, Inst. Phys. Ser. No. 87, p. 703 (1987).

Appendix G

Depletion Zone Limited in Si-$TaSi_2$ Eutectic Composites

Depletion zone limited transport in Si-$TaSi_2$ eutectic composites

B. M. Ditchek, B. G. Yacobi, and M. Levinson
GTE Laboratories, Inc., 40 Sylvan Road, Waltham, Massachusetts 02254

(Received 22 June 1987; accepted for publication 9 November 1987)

Depletion zones surrounding aligned, cylindrical, metal-semiconductor junctions formed during the directional solidification of a eutectic mixture are shown to influence the transport properties of the composite. Hall-effect and direct depletion zone width measurements made using the electron beam induced current technique of the scanning electron microscope have demonstrated that a relatively small total volume fraction ($\sim 10\%$) of depleted material can lead to a significant increase in resistivity. The sensitivity of the resistivity of the composite to the depleted zone volume is attributed to a cellular distribution of the $TaSi_2$ rods which causes substantial current streamlining. An analysis of the dopant segregation that occurs in the Si matrix of the composite boule during solidification supports the depletion zone limited transport model. The dependence of the resistivity on the depleted zone volume fraction of the composite indicates that the switching action in this novel material is achievable by increasing the volume fraction of depleted material between a source and drain contact.

I. INTRODUCTION

Semiconductor-metal eutectic (SME) composites comprise an interesting new class of electronic materials. The unique microstructure exhibited by these composites consists of aligned arrays of metallic rods embedded in a semiconducting matrix. At each rod-matrix interface a cylindrical rectifying junction is formed. Consequently, the electronic structure can be depicted as a three-dimensional or "volumetric" aligned array of Schottky junctions and is suggestive of several new and potentially advantageous applications.

High-power switching is one example of an application in which the volumetric character of SME materials appears to offer distinct advantages. As envisioned in a SME switching device, current flows through the volume of the material perpendicular to the rods. Switching action is obtained when the semi-insulating depletion zones associated with the Schottky junctions are expanded to the point of overlap by the application of a sufficiently large reverse-bias voltage to the rods. In the unbiased state, the depletion zones occupy only a small volume fraction of the semiconducting matrix and the resistivity of the device is determined by the bulk resistivity of the semiconducting phase. The application of a reverse-bias voltage causes the depletion zones to expand and eventually interpenetrate. With a bias the depletion-zone volume fraction approaches unity and the resistivity of the material increases by orders of magnitude.

Semiconductor-metal eutectic composites displaying a rodlike microstructure have been prepared by directional solidification in Ge, Si, and several III-V based systems. Helbren and Hiscocks surveyed several Ge- and Si-based eutectics.[1] Reis and Renner similarly prepared GaAs-based eutectics.[2] Until recently, however, very little work has been done on the electrical and electronic properties of these materials. Levinson examined the electrical resistivity of a silicon-silicide eutectic.[3] He observed a significant anisotropy in the resistivity of the Si-$CrSi_2$ composite due to the alignment of the rods along the growth axis. A similar anisotropy has been found in the Ge-$TiGe_2$ eutectic.[4] This investigation considered the effect of depletion zones surrounding the rods on the transport in the semiconductor perpendicular to the rod axis for the first time. The anomalously high resistivity observed at low temperatures, however, was shown to be unrelated to the depletion zones; the effect was traced to structural defects, such as grain boundaries and dislocations in the polycrystalline Ge matrix.[4,5]

Recently, interest in the electronic properties of semiconductor-metal eutectic composites has been heightened by the availability of materials with single-crystal matrices. Particular attention has been focused on Si-$TaSi_2$ composites. Transport measurements have shown that the carrier concentration in the Si matrix of these composites can be controlled by doping the melt. Electron and hole mobilities have been found to be typical of the values expected for single-phase, single-crystal Si. The grown-in metal-semiconductor junctions have been characterized by current-voltage (I-V) and capacitance-voltage (C-V) techniques and shown to display nearly ideal diode characteristics. The Schottky barrier height of the grown-in $TaSi_2$ n-type Si junction was found to be 0.62 eV.[6] Electron beam induced current (EBIC) analysis has demonstrated graphically the presence of a depletion zone around each $TaSi_2$ rod and has provided a measurement of the depletion-zone width as a function of voltage.[7] In addition, the presence of deep levels in the Si matrix due to Ta was investigated using deep-level transient spectroscopy (DLTS). No electrically active Ta was detected indicating that the concentration does not exceed the minimum experimental sensitivity of 6×10^{11} cm^{-3} (Ref. 8). Together these studies have established that the material and electronic properties of the Si-$TaSi_2$ system are suitable for the development of electronic devices.

Device applications invariably involve the transport of current through the material. In this report the influence of the cylindrical depleted regions surrounding the rods on the resistivity of a semiconductor-metal eutectic composite is established. The results are interpreted in the context of the

 0021-8979/88/061964-07$02.40

growth history, microstructure, and other transport properties of the Si-$TaSi_2$ eutectic.

II. EXPERIMENTAL METHODS

A. Composite growth

The composites were prepared by directional solidification via Czochralski crystal growth techniques using a (111)Si seed and a crucible charged with Wacker float-zone Si and Gallard–Schlesinger float zone Ta of 99.996% purity. The crystal growth system has been used previously to grow single-crystal Ge-matrix eutectic composites and is based on rf induction heating of a graphite susceptor lined with a quartz crucible.[5] Although the composite could be grown with either *p*- or *n*-type matrix, most of the studies were performed on boules with a P doped, *n*-type Si matrix. This choice was made based on the earlier observations of a high Schottky barrier of 0.62 eV at the *n*-type Si/$TaSi_2$ *in situ* junctions.

Optimization of the growth technique has resulted in eutectic composites with grain-boundary-free Si matrices with the same (111) orientation as the Si seed. The yield of quasi-single-crystal composites depends sensitively on the ability to solidify from the exact eutectic composition of Si—5.5 wt. % Ta. Although growth rates between 2 and 20 cm/h have been used, the yield of quasi-single crystals is much greater for growth rates at the upper end of this range. Composites grown at rates above 20 cm/h tend to degenerate into a dendritic, polycrystalline structure. All the electrical measurements were performed on samples prepared from boules with a single-crystal (111)Si matrix.

B. Electrical measurements

The electrical transport properties of the composites have been characterized by resistivity, Hall-effect, and EBIC measurements. The resistivity and Hall coefficient measurements were performed on standard bridge-type samples ultrasonically cut from grain-boundary-free Si-$TaSi_2$ wafers sliced perpendicular to the (111) growth direction. Samples were 0.64 mm thick. The rods which run parallel to the growth direction were oriented perpendicular to the plane of the wafer. All resistivities reported in this paper for the anisotropic composite are perpendicular resistivities, measured with current flow perpendicular to the rods. Resistivity and Hall measurements were made on several wafers selected from different positions along the boule. The volume fraction of the boule solidified to that point, f_s, was calculated for each wafer. The Hall carrier concentrations were plotted as a function of position in the boule, as in Fig. 5, so that wafers with a known value of f_s could be assigned a Hall carrier concentration and then be used for other measurements. The Hall carrier concentrations reported in Sec. IV B for wafers in which diodes were fabricated and EBIC measurements were made were obtained in this way.

Contacts to the Hall samples were formed by evaporating Au-Sb films on the *n*-type wafers and annealing at 400 °C. All measurements were performed with a 6-kG magnetic field parallel to the rod axis and the electric field perpendicular to the rod axis. In this geometry, both the current and Hall voltage were perpendicular to the rod axis.

In addition to the Hall measurements, it is desirable to have an independent measure of the carrier concentration in the Si matrix between the rods. The EBIC technique can provide such a measurement.[7] To extract a value of the carrier concentration from EBIC data, EBIC measurements of the depletion zone width W as a function of reverse-bias voltage V_r are compared to W vs V_r curves calculated for different carrier concentrations from Poisson's equation. The carrier concentration giving the best fit to the data are considered a measure of the actual matrix carrier concentration n and are denoted n_{EBIC} to label the procedure used to generate the value. This technique was utilized to obtain the Si matrix carrier concentration over a wide range of carrier concentrations.

The EBIC measurements required the fabrication of diodes that utilize the *in situ* junctions in the composite. The same diode contact procedures used in the original EBIC studies were repeated here.[6,7] Briefly, contacts were made to the $TaSi_2$ rods by the formation of a 0.2-μm-thick surface metallic film of $CoSi_2$. This film provided a Schottky contact to the Si but an ohmic contact to the rods. Ohmic contacts were formed at the edges of the wafers by the deposition and alloying of a Au-Sb film. EBIC observations were made on the face of the wafer opposite the $CoSi_2$ contact.

III. MICROSTRUCTURE

The microstructure of the Si-$TaSi_2$ eutectic composite is similar to the idealized structure discussed in the introduction: an aligned array of metallic $TaSi_2$ rods in a Si matrix. The eutectic composition corresponds to about 2 vol % of the $TaSi_2$ phase in Si. A micrograph of a polished surface of a composite grown at 20 cm/h is shown in Fig. 1. The rodlike structure of the $TaSi_2$ phase is evident in Fig. 2, which shows a polycrystalline wafer of the composite after the Si matrix has been etched back in NaOH/NaOCl solution.

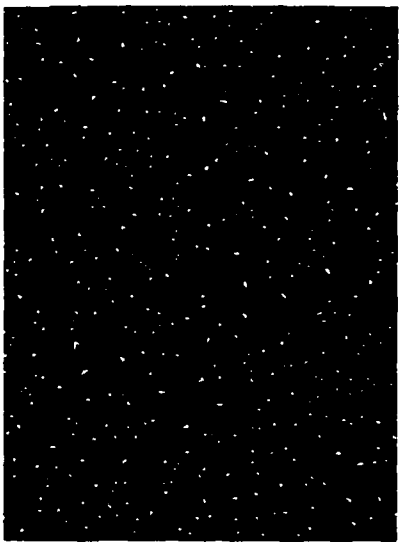


FIG. 1. A scanning electron micrograph of a transverse Si-$TaSi_2$ eutectic wafer.

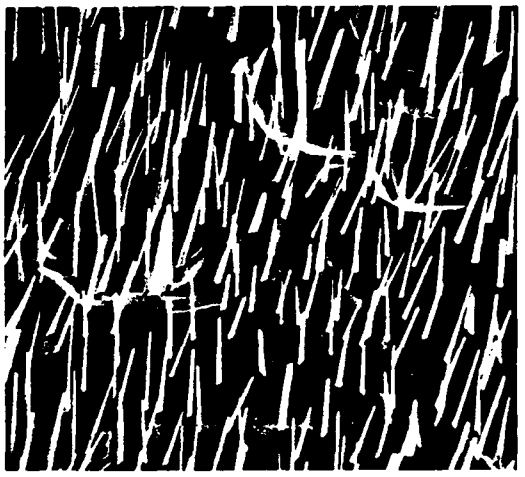


FIG. 2. A scanning electron micrograph of a transverse Si-$TaSi_2$ eutectic wafer after etching the Si surface to reveal the $TaSi_2$ rods.

According to models of eutectic solidification, the interrod spacing λ depends on the growth rate according to

$$\lambda = Av^{-1/2}, \tag{1}$$

where A is a constant for a particular eutectic system and v is the growth rate.[9] The interrod spacing has been measured over the range of accessible pull rates (2–20 cm/h) by determining the rod density N_r and defining

$$\lambda = (N_r)^{-1/2}. \tag{2}$$

This definition establishes λ as an average interrod spacing. The results are shown in Fig. 3. It is clear that over this limited range of growth rates, the data are consistent with Eq. (1) with $A = 6.0 \pm 0.8 \times 10^{-5}$ $cm^{3/2}\,s^{-1/2}$. For the composite grown at 20 cm/h and shown in Fig. 1, the rod density is 1.6×10^6 rods/cm^2 and $\lambda = 7.9$ μm. No attempt has been made to correct the growth rate for the change in melt level during growth or for the occasional changes due to adjustments in the rf power level needed to control the boule diameter. This accounts for some of the scatter observed in these data.

Within a given transverse plane of a boule, variations in rod density and therefore, interrod spacing, are small; values of N_r measured over areas containing about 100 rods vary only by about 2%. Comparisons of N_r in boules grown at the same pull rate and in different wafers within the same boule, however, reveal fluctuations of as much as $\pm$ 15%.

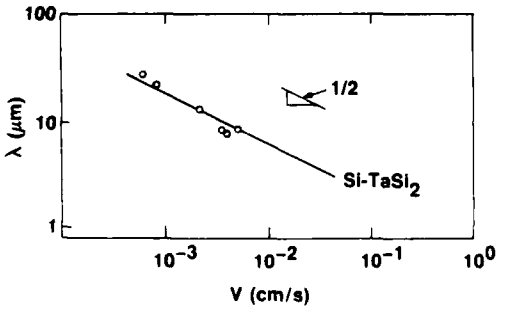


FIG. 3. The dependence of the interrod spacing on the growth rate.

The length of the rods has been previously investigated using EBIC techniques. Although the maximum length was not established, it was verified that all the rods do run continuously through wafers 1.25 mm thick, approximately twice the thickness of the Hall samples.[7]

The typical transverse section displayed in Fig. 1 shows that rods in the eutectic are neither arranged in a regular latticelike array nor distributed in a strictly random pattern. Examination of many such sections has revealed a kind of cellular structure. The interrod spacing in the cell walls is less than the average interrod spacing given by Eq. (2). For the case of an average interrod spacing of 7.9 μm, the rods in the cell walls have an average spacing of $\sim$4.5 μm. The interior of the cells exhibits a very low rod density and covers an area with a diameter several times the average interrod spacing. The cellular nature of the rod distribution will be shown to be important in analyzing the effect of depletion zones on transport in these composites.

Many of the $TaSi_2$ rods are not circular in cross section, but are faceted. Some displayed the arrowhead shape observed by Helbren and Hiscocks in the Si-$NbSi_2$ eutectic.[1] The degree of anisotropy in rod cross section decreases as the growth rate is increased from 2 to 20 cm/h. Thus, in the high rod density composites of interest in this study, the deviation of the rods from a circular cross section is minimal.

IV. TRANSPORT MEASUREMENTS

A. The resistivity and Hall effect analysis

The resistivity of an n-type semiconductor is

$$\rho = (q\mu n)^{-1}, \tag{3}$$

where μ is the mobility, n is the carrier concentration, and q is the unit of elementary charge. If an array of aligned metallic rods is embedded in the semiconductor, then the resistivity of the composite structure will not, in general, be the same as the resistivity of its semiconducting matrix. Each rod will be surrounded by a semi-insulating depletion zone as a consequence of the Schottky barrier established by the metal/n-type semiconductor junction. The depletion zone will isolate the rod from the matrix. Therefore, the material can be considered to be a composite of a semiconductor and a semi-insulator, rather than a semiconductor and a metal.

The perpendicular resistivity (i.e., current flow perpendicular to the rod axes) of such a composite material will depend on the fraction of the volume occupied by the semi-insulating material and metallic rods, ϵ. In the limit of small ϵ, the composite resistivity will be nearly unaffected by the depleted zones and the resistivity of the composite will be similar to that of the semiconductor. If the depleted volumes expand to the point where the semiconducting regions are no longer interconnected, then the resistivity of the composite will be orders of magnitude higher than the resistivity of the semiconductor.

The following analysis of the transition from one limit to the other is based on Read's analysis of the resistivity and Hall effect of a semiconductor with an array of parallel space charge cylinders in a semiconducting matrix.[10] Read concluded that the space-charge cylinders can affect transport by (i) scattering directly from the space-charge cylinders,

(ii) a reduction in the average concentration of charge carriers, and (iii) a distortion of current streamlines.

The first effect is negligible in the present case because the average interrod spacing is orders of magnitude larger than the electron mean-free path. Hence, the actual mobility of the electrons will not be affected by the depleted zones around the rods. The second effect can be related directly to the fraction of the composite occupied by the depleted volume. In a composite with rods of radius r_0 and a rod density, N_r,

$$\epsilon = \pi(r_0 + W)^2 N_r. \tag{4}$$

The average carrier concentration is given by

$$\langle n \rangle = n(1 - \epsilon). \tag{5}$$

Read included the final effect of current streamlining around the space-charge cylinders by defining the function

$$g(\epsilon) = \langle E_x \rangle_n / \langle E_x \rangle, \tag{6}$$

where the x direction is the direction of current flow, $\langle E_x \rangle_n$ is the electric field in the x direction averaged over the normal n-type material between the space-charge cylinders, and $\langle E_x \rangle$ is the applied electric field in the x direction averaged over the entire composite volume. In the limit of very small ϵ, $g(\epsilon) = 1$. However, when ϵ approaches unity and adjacent depletion zones overlap, the voltage drop occurs primarily over the depleted volume and $g(\epsilon)$ approaches 0. The actual functional dependence of $g(\epsilon)$ on ϵ will depend on the details of the distribution of space-charge cylinders. Read has shown that when ϵ is small, a regular lattice of space-charge cylinders will yield $g(\epsilon) \sim 1 - \epsilon$.

In such a composite, the current density averaged over the entire composite volume, $\langle J_x \rangle$,is given by

$$\langle J_x \rangle = q\mu \langle n \rangle \langle E_x \rangle_n. \tag{7}$$

In terms of the measurable quantity $\langle E_x \rangle$ and the semiconductor-matrix carrier concentration n,

$$\langle J_x \rangle = q\mu n(1 - \epsilon)g(\epsilon)\langle E_x \rangle. \tag{8}$$

Thus the composite resistivity ρ_c is

$$\rho_c^{-1} = q\mu n(1 - \epsilon)g(\xi). \tag{9}$$

The composite resistivity relative to the resistivity of the semiconductor matrix is

$$\rho_c/\rho = [(1 - \epsilon)g(\epsilon)]^{-1}. \tag{10}$$

Hence, the increase in resistivity due to depletion-zone-limited transport will depend on the form of $g(\epsilon)$, a function predominantly affected by the geometric distribution of the space-charge cylinders, or in this case, the $TaSi_2$ rods. For a regular hexagonal array of depleted cylinders, Read showed that $g(\epsilon) \sim (1 - \epsilon)$ when ϵ is small.

Read also showed that the Hall effect, performed with the magnetic field along the axis of the space-charge cylinders will yield the Hall parameters, n_H and μ_H which are related to the actual n and μ of the semiconductor matrix material by

$$n = n_H[(1 - \epsilon)g(\epsilon)]^{-1} \tag{11}$$

and

$$\mu = \mu_H. \tag{12}$$

The mobility determined from the Hall effect represents the physical mobility of electrons in the semiconducting matrix. However, the carrier concentration derived from the Hall effect will actually underestimate the semiconductor-matrix carrier concentration by the factor $(1 - \epsilon)g(\epsilon)$. Consequently, when ϵ is small, the Hall effect should yield a carrier concentration approximately equal to the carrier concentration in the semiconductor matrix. When ϵ is large, however, the Hall effect will yield a much lower carrier concentration than the actual carrier concentration of the semiconductor matrix, indicative of the depletion zones causing a significant increase in the composite resistivity.

B. Depletion-zone effects

The above analysis indicates that to determine the effect of the depletion zones on the resistivity of the composite it is necessary to measure both n_H and n. The actual concentration of carriers in the Si matrix n can be measured using the EBIC mode of the scanning electron microscope as outlined in Sec. II B. In this technique, EBIC is used to determine the depletion-zone width over a range of bias voltages for a given diode. The depletion zone–bias voltage relationship (W-V_r) calculated from Poisson's equation in cylindrical coordinates is fit to the EBIC data using the carrier concentration as an adjustable parameter. Poisson's equation yields

$$\{(r_0 + W)^2 - r_0^2 - 2(r_0 + W)^2 \ln[(r_0 + W)/r_0)]\} = -4\epsilon_s/qn(V_b + V_r), \tag{13}$$

where with ϕ_b as the Schottky barrier height, $V_b = \phi_b/q$, V_r is the reverse bias voltage, and ϵ_s is the dielectric constant of the semiconductor. The solid lines in Fig. 4 show the theoretical W-V_r curves over a wide range of carrier concentrations for a 1.0-μm-diam rod and a Schottky barrier height of 0.62 eV. The calculation indicates that the depletion zone width around a metallic rod is very sensitive to the carrier concentration. Also plotted in this figure are the EBIC measurements of W vs V_r for two different samples with significantly different Hall carrier concentrations, but nearly identical interrod spacing. Fitting the theoretical curves to the experimental data provides n_{EBIC}, which, since it depends

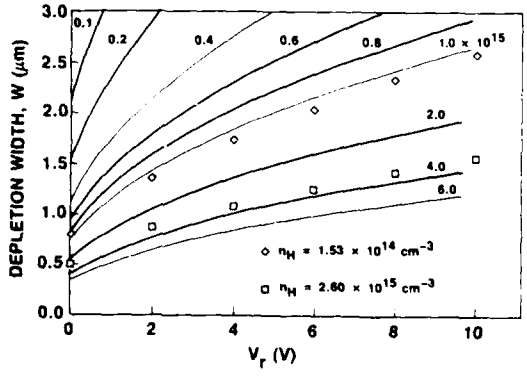


FIG. 4. The dependence of the depletion-zone width (W) on the applied reverse-bias voltage (V_r). The rod diameter is 1.0 μm. The solid lines represent the theoretical relationship calculated from Eq. (13) for different Si-matrix carrier concentrations. The points correspond to EBIC measurements made on two different wafers of widely differing Hall carrier concentration.

only on the carrier concentration between the rods, is a measure of n.

Depletion zone width measurements in the wafer with $n_H = 2.6\times10^{15}\,\mathrm{cm}^{-3}$ yielded $n_{EBIC} = 3.6\times10^{15}\,\mathrm{cm}^{-3}$. The agreement between n_H and n_{EBIC} is good for this carrier concentration range. In contrast, measurements in the wafer with $n_H = 1.5\times10^{14}\,\mathrm{cm}^{-3}$ gave $n_{EBIC} = 1.1\times10^{15}\,\mathrm{cm}^{-3}$. This difference is too large to be explained by uncertainties in the depletion-zone measurement. For example, if $n = 1.5\times10^{14}\,\mathrm{cm}^{-3}$, then the unbiased depletion width should be 1.75 μm, a value more than twice the 0.8 μm measured. At a 10-V reverse bias the difference between the expected and measured value becomes 4.25 μm. The divergence of n_H and n_{EBIC} at low carrier concentrations is significant and reflects the increase in resistivity due to depletion zone limited transport.

The ratio n_{EBIC}/n_H, which reflects the relative increase in resistivity caused by the depletion zones, is plotted versus n_{EBIC} in Fig. 5. These data show that when n_{EBIC} exceeds $2\times10^{15}\,\mathrm{cm}^{-3}$ and ϵ is less than about 0.05, the depletion zones have a minimal effect on resistivity. Below $n_{EBIC} = 2\times10^{15}\,\mathrm{cm}^{-3}$, however, ϵ becomes sufficiently large to cause the composite resistivity to significantly exceed that of the semiconductor matrix. Since the maximum value observed for ϵ is only 0.1, the analysis suggests that it is $g(\epsilon)$, or the current streamlining effect, that is primarily responsible for the increase in resistivity.

Also plotted in Fig. 5 is the Read approximation for small vaues of ϵ of $n/n_H = (1-\epsilon)^{-2}$. Comparison of the data with the theoretical $(1-\epsilon)^{-2}$ curve shows that the increase in resistivity occurs at a much higher carrier concentration than would be expected for the close packed, regular distribution of rods considered by Read. The reasons for this will be discussed in Sec. V.

The carrier concentration data are compiled in Table I along with data on wafer resistivity, electron mobility, and the unbiased depletion-zone width. Despite the significant increase in resistivity at low carrier concentration, the Hall electron mobility, as expected from Read's analysis, is unaffected. The table also includes a calculation of $g(\epsilon)$ based on Eq. (11).

C. Segregation analysis

The carrier concentration within a given Si-$TaSi_2$ eutectic boule increases systematically from the seed end to the tail end. The axial profile of the carrier concentration of numerous boules have been analyzed according to the expected segregation of dopants during Czochralski growth. The analysis provides additional support for the interpretation of the Hall and EBIC carrier concentrations and, therefore, for the observations of depletion zone limited transport.

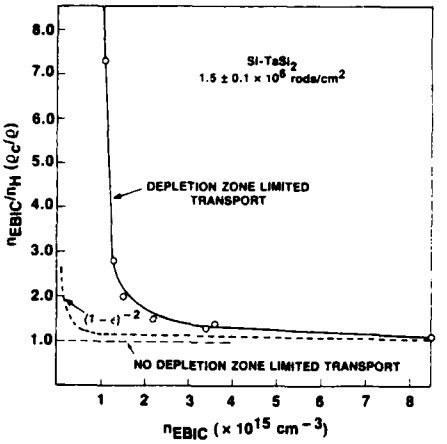


FIG. 5. Correlation of the EBIC and Hall carrier concentration ratio (n_{EBIC}/n_H) [equivalently the ratio of composite to matrix (ρ_c/ρ)] as a function of the matrix carrier concentration n_{EBIC}. The significant increase in this ratio below $2\times10^{15}\,\mathrm{cm}^{-3}$ is due to depletion zone limited transport.

In a Czochralski-grown boule, the axial distribution of a dopant having a segregation coefficient k is given by

$$C_s = kC_0(1-f_s)^{k-1}, \tag{14}$$

where C_0 is the initial melt concentration of the dopant, C_s is the dopant concentration in the solid, and f_s is the volume fraction of the boule solidified.[11] The segregation coefficient of the P dopant in Si is 0.35.[12] Segregation analysis is usually performed using the Hall effect to measure the concentration of the shallow dopant assuming temperatures are sufficiently high to ionize the shallow donor levels and no deep levels are present that might compensate the donors. In the case of eutectic boules, deep levels associated with Ta have previously been shown to be too low[8] to affect the relationship between carrier concentration and P concentration. A plot of $\log n_H$ vs $\log(1-f_s)$ yields a straight line with a slope of $k-1$ if Eq. (14) is obeyed.

The phosphorous concentration C_s has been determined as a function of f_s from Hall measurements on the eutectic boules and on a control boule of P-doped single-

TABLE I. Depletion zone limited transport.

Sample[a,b]	ρ_c (Ω cm)	μ_H (cm²/V s)	n_H (×10¹⁵ cm⁻³)	n_{EBIC} (×10¹⁵ cm⁻³)	$\frac{n_H}{n_{EBIC}}\frac{(\rho_c)}{\rho}$	ϵ	$g(\epsilon)$
1	1.0	800	7.50	8.50	1.1	0.040	0.9
2	2.9	820	2.60	3.40	1.3	0.045	0.81
3	3.0	830	2.50	3.60	1.4	0.045	0.73
4	4.4	940	1.50	2.20	1.5	0.060	0.71
5	9.0	900	0.77	1.50	1.9	0.085	0.58
6	15.7	950	0.42	1.25	3.0	0.090	0.37
7	44.6	935	0.15	1.10	7.3	0.10	0.15

[a] Wafers from three different boules.
[b] $N_r = 1.4$–1.6×10^6 rods/cm².

phase Si grown in the same crystal puller. Phosphorous segregation in the control boule obeyed Eq. (14) and analysis yielded a segregation coefficient in good agreement with the accepted value of 0.35. In contrast, all the Si-$TaSi_2$ eutectic boules exhibited anomalous results.

Figure 6 depicts the analysis of a typical eutectic boule. Curves of n_H vs $\log(1-f_s)$ exhibit pronounced nonlinear slopes varying from -0.65 at the seed end of the boule to values in excess of -1 at the tail. Although k might differ from the accepted value of 0.35 due to the high concentration of Ta in the eutectic melt, the inability of Eq. (14) to describe the Hall data suggests that the measurement does not accurately determine the P concentration in these materials. Better agreement with Eq. (14) might be obtained by using n_{EBIC} in place of the Hall-derived n_H. The results in Table I can be used to convert the Hall data to the actual carrier concentration derived from EBIC. The corrected data plotted in Fig. 6, does yield the expected straight line but with a segregation coefficient of 0.5.

Segregation analyses of several other eutectic boules has yielded segregation coefficients between 0.4 and 0.7. This variation in the segregation coefficient is an artifact; the segregation mode is not varying from boule to boule. The range of segregation coefficients is traceable to small variations in the boule-rod density and distribution. The relationship between n_H and n_{EBIC} in Fig. 5 and Table I is specific to composites with a rod density of $1.5 \pm 0.1 \times 10^6$ cm^{-2}. The segregation analysis can only be made for wafers within this limited rod density range because the relationship between n_H and n_{EBIC} is very sensitive to N_r. A rod density exceeding 1.5×10^6 cm^{-2} will lead to an increase of n_{EBIC}/n_H at a higher value of n_{EBIC}; similarly, a lower rod density will cause the ratio to significantly exceed one at a lower value of n_{EBIC}. Furthermore, the rod distribution may significantly affect the conversion factor between n_H and the actual carrier concentration. In light of the observed variations in rod density noted in Sec. III, the observed uncertainty in k is not surprising. The segreation analysis clearly indicates that n_{EBIC} is a more accurate measurement of the dopant concentration than is n_H and is further evidence of the validity of the depletion-zone-limited transport analysis presented in this paper.

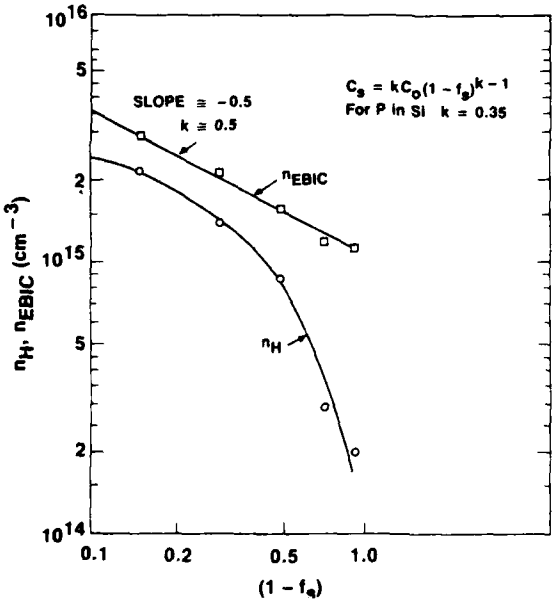


FIG. 6. A segregation analysis of the P dopant in the composite boule using both Hall and EBIC carrier concentrations.

V. DISCUSSION

The analysis presented in Sec. IV demonstrates that the depletion zones surrounding the $TaSi_2$ rods in the Si-$TaSi_2$ eutectic composite can influence the resistivity of the composite. Composites with rod densities of 1.5×10^6 rods/cm^2 and depletion-zone widths less than $\sim 0.5\,\mu$m ($n \geqslant 3.5 \times 10^{15}$ cm^{-3}) exhibit a resistivity approximately that of the semiconductor matrix. Composites with a similar rod density, but with depletion zone widths exceeding $\sim 0.8\,\mu$m ($n \leqslant 1.3 \times 10^{15}$ cm^{-3}), display a significantly increased resistivity caused primarily by current streamlining. It is expected that similar changes in resistivity can be obtained by expanding the depletion-zone size with a bias voltage.

The results of the analysis are in reasonable agreement with the Read model although the onset of the resistivity increase occurs at a much smaller value of ϵ than expected for a regular hexagonal array of space-charge cylinders. The Si-$TaSi_2$ eutectic microstructure shown in Fig. 1 is clearly not composed of a regular close packed distribution of metal rods. The current streamline function $g(\epsilon)$ is very sensitive to the details of the distribution of space-charge cylinders. Read[10] discussed the form of $g(\epsilon)$ and showed the results of resistance measurements made on a resistive film with a regular hexagonal array of holes as a function of the diameter of the holes. For this close-packed distribution, interpenetration of the depletion zones, or pinch-off of current flow, occurs when $\epsilon = 0.91$.

Presumably, it is the absence of a close-packed, regular distribution of rods that causes $g(\epsilon)$ for the eutectic system to decrease so rapidly at small values of ϵ. The rods tend to segregate into the walls of a cellular structure with an average interrod spacing in the walls of $\sim 4.5\,\mu$m. For such a cellular structure, the packing of rods is open and the value of W and ϵ that results in current pinch-off is reduced from that expected from the average interrod spacing given by Eq. (2). Consider, for example, the arrays of rods in Fig. 7. The dimensions of all the structures are such that the average rod density is 1.6×10^6 rods/cm^2. For the square array inherent in the assumption behind Eq. (2), $\lambda = 7.9\,\mu$m. Hence, for an average 1.2-μm-diameter rod, corresponding to the eutectic composition, interpenetration of the depletion zones occur at $W = 3.35\,\mu$m or $\epsilon = 0.785$. For the close packed hexagonal array discussed above, $g(\epsilon) = 0$ at $W = 3.65\,\mu$m or $\epsilon = 0.91$. As the packing density is reduced to the structure denoted as a 3-hex cell, the spacing between rod centers in the wall is 4.6 μm and $g(\epsilon) = 0$ when $W = 1.72\,\mu$m and $\epsilon = 0.27$. Thus, depending on the packing of the rods, $g(\epsilon)$ can go to zero when ϵ is small.

Because the average interrod spacing in the walls of the cell structure is $\sim 4.5\,\mu$m, it is probable that pinch-off will result at a similarly small value of the depletion-zone volume fraction. The variation of the interrod spacing in the wall may also result in a more gradual drop in $g(\epsilon)$ relative to

ARRAY[a]		g(ϵ) = 0 for W (μm)	ϵ
1. Square	7.9	3.35	0.79
2. Hexagonal	8.5	3.65	0.91
3. Simple Hex	7.0	2.90	0.78
4. 2-Hex Cell	5.5	2.15	0.38
5. 3-Hex Cell	4.6	1.72	0.27

[a] Dimensions in microns

FIG. 7. The effect of rod distribution on the values of the depletion-zone width (W) and depletion-zone volume fraction (ϵ) necessary to obtain pinch-off. The array dimensions correspond to $N_r = 1.6\times10^6$ rods/cm^{-2}.

that expected for a regular distribution. Therefore a significant increase in resistivity should be evident, even when ϵ is significantly less than the value needed for pinch-off. The discussion is intended to clarify the relationship between $g(\epsilon)$ and the rod distribution; a theoretical derivation of $g(\epsilon)$ would require a reasonable mathematical model of the rod distribution function.

VI. CONCLUSION

The influence of depletion zones on current transport in a semiconductor metal-eutectic composite has been established. It was found that the resistivity of the composite is essentially that of the matrix when the depletion-zone volume fraction is less than 0.05. Further, it was shown that the resistivity increases significantly relative to that of the matrix when the depletion zone volume fraction is raised to 0.1. The sensitivity of the resistivity to a relatively small fraction of depleted volume is a consequence of the open, cellular distribution of the rods. The observation of depletion-zone-limited transport in these composites indicates that switching action in this material can be realized by manipulating the depletion-zone volume fraction via a bias voltage applied to the rods.

ACKNOWLEDGMENTS

The authors wish to thank T. Middleton for his assistance in the growth of the composites and fabrication of the devices. Helpful discussions and a critical review of the manuscript by Dr. J. Gustafson are also gratefully noted. Research was sponsored by the Air Force Office of Scientific Research (AFSC), under Contract No. F49620-86-C-0034. The United States Government is authorized to reproduce and distribute reprints for governmental purposes notwithstanding any copyright notation hereon.

[1] N. J. Helbren and S. E. R. Hiscocks, J. Mater. Sci. **8**, 1744 (1973).
[2] B. Reiss and T. Renner, Z. Naturforsch. A **21**, 546 (1966).
[3] L. M. Levinson, Appl. Phys. Lett. **21**, 289 (1971).
[4] B. M. Ditchek, J. Appl. Phys. **57**, 1967 (1985).
[5] B. M. Ditchek, J. Cryst. Growth. **75**, 264 (1986).
[6] B. M. Ditchek and M. Levinson, Appl. Phys. Lett. **49**, 1656 (1986).
[7] B. G. Yacobi and B. M. Ditchek, Appl. Phys. Lett. **50**, 1083 (1987).
[8] M. Levinson, B. M. Ditchek, and B. G. Yacobi, Appl. Phys. Lett. **50**, 1906 (1987).
[9] W. A. Tiller, *Liquid Metals and Solidification* (American Society for Metals, Cleveland, OH, 1958), p. 276.
[10] W. T. Read, Jr., Philos. Mag. **46**, 111 (1955).
[11] M. C. Flemings, *Solidification Processing* (McGraw-Hill, New York, 1974).
[12] J. Keenan and G. B. Larrabee, in *VLSI Electronics*, edited by N. G. Einspruch and G. B. Larrabee (Academic, New York, 1983), pp. 2–72.

Appendix H

Novel High Voltage Transistor Fabricated Using the *In Situ* Junctions in a Si-$TaSi_2$ Eutectic Composite

Novel high voltage transistor fabricated using the *in situ* junctions in a Si-$TaSi_2$ eutectic composite

B. M. Ditchek, T. R. Middleton, P. G. Rossoni, and B. G. Yacobi
GTE Laboratories, Inc., 40 Sylvan Road, Waltham, Massachusetts 02254

(Received 10 December 1987; accepted for publication 2 February 1988)

Transistor action has been observed for the first time in a Si-$TaSi_2$ eutectic composite. These devices, utilizing the *in situ* cylindrical Schottky junctions between the Si matrix and the $TaSi_2$ rod phase, have characteristics typical of a metal-semiconductor field-effect transistor (MESFET). However, unlike a conventional planar device like a MESFET, eutectic transistors are resistant to avalanche breakdown. A device is demonstrated that blocks 600 V, a value that is three times larger than would be expected for a planar device of the same carrier concentration.

Directional solidification of eutectic mixtures can yield a composite material with a rodlike or lamellar distribution of phases. The aligned structures produced by the directional solidification of semiconductor-semiconductor[1,2] or semiconductor-metal[3,4] eutectic systems have long been considered to hold great promise for electronic devices benefiting from a three-dimensional distribution of *p-n* or Schottky junctions. Nevertheless, significant progess was slow to achieve primarily because of problems growing electronic quality material and in characterizing the two phase materials. Recently, however, a eutectic composite material of semiconducting Si with aligned metallic rods of $TaSi_2$ has been shown to contain *in situ* Schottky junctions in a single-crystal matrix of good electronic quality.[5-7] Using these junctions nearly ideal diodes and efficient photodiodes have been fabricated.[5,8] The microstructural and electronic properties of this material have indicated that it also might be used to fabricate field-effect transistors.[5-9]

It is the purpose of this letter to demonstrate that eutectic composite substrates can be used to fabricate field-effect transistors and to characterize these initial devices.

Transistor action in this material depends on using the *in situ* Schottky junctions at the interface between the metallic phase and the semiconducting phase to control the flow of current between a source and a drain. The eutectic composite material possesses the basic requirements for such a device. The composite can be grown with a low *n*-type carrier concentration in a single crystalline Si matrix.[5] The rods can be spaced such that the depletion zones around the rods can be expanded to the point of overlap with a small reverse bias voltage.[6] Finally, electron beam induced current studies have indicated that the rods run continuously through the thickness of a wafer and should therefore provide a complete barrier to the flow of current.[9]

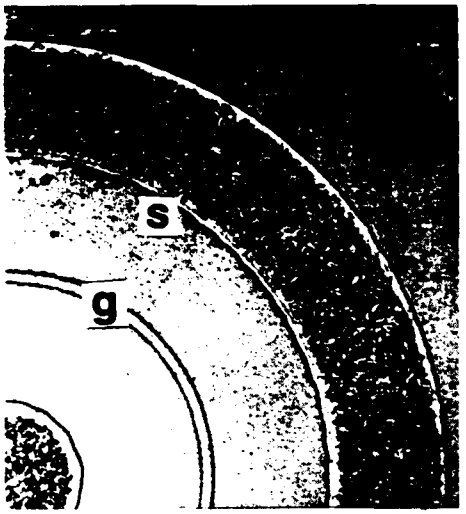
Boules, approximately 2 cm in diameter, were pulled from a melt with the eutectic composition, Si 5.5 wt. % Ta, at a rate of 20 cm/h to yield a composite with about 2×10^6 rods/cm^2. The Si was phosphorus doped to a level of about 10^{15} cm^{-3}. Wafers were cut transverse to the growth direction and had the $TaSi_2$ rods running through its thickness normal to the plane of the section. A simple concentric ring design was used for the contacts. As shown in Fig. 1(a), the outside ring acted as the source and the inside dot as the drain. Current moving from the source to the drain passes under the centrally located gate contact.

In the first fabrication step, the wafers were thermally oxidized at 1000 °C to grow a 0.3-μm-thick oxide. Vias in the oxide were opened for the surface contacts. The gate contact was formed by the direct silicidation of an evaporated Co film at 800 °C to form a surface film of $CoSi_2$. The silicide forms an ohmic contact to the $TaSi_2$ gate rods and a rectifying contact to the Si matrix. Figure 1(b) shows a scanning electron micrograph of the $CoSi_2$ gate contact film with the $TaSi_2$ beneath it. The source and drain contacts were fabricated using annealed, evaporated Au-Sb films. In certain cases, $CoSi_2/n^+$ contacts were used for the source and drain. The distribution of the rods in the composite substrate and, particularly, under the narrow gate region, does not exhibit lithographic regularity. Devices were fabricated with gate contact widths varying between 20 and 125 μm.

A determination of the carrier concentration of the Si matrix was performed using the Hall effect and electron beam induced current (EBIC) measurements. As discussed in earlier work, while the Hall effect underestimates the Si matrix carrier concentration, using EBIC to fit a curve of the depletion zone width around a rod with reverse bias voltage provides a much more accurate determination of the carrier concentration.[7,9] It is this technique that is used to specify the Si matrix carrier concentration for the wafers used in this study.

An example of the current-voltage characteristics of a eutectic composite transistor with the drain current plotted against the drain voltage for different gate voltages is shown in Fig. 2. The carrier concentration of the Si matrix of this device is 2×10^{15} cm^{-3} and the resistivity of the composite along the direction perpendicular to the rod axis is 20 Ω cm. The substrate is 250 μm thick and has the surface contact dimensions shown in Fig. 1. The basic characteristics of the device are similar to those of a conventional metal-semiconductor field-effect transistor (MESFET) in that they display a linear region and a saturation region.[10] The series resistance of the device, taken as the slope of the unbiased curve in the limit of small drain voltages, is 400 Ω. In light of the composite resistivity and the device dimensions, this value indicates that the entire thickness of the device is being used for the current channel.

 0003-6951/88/141147-03$01.00



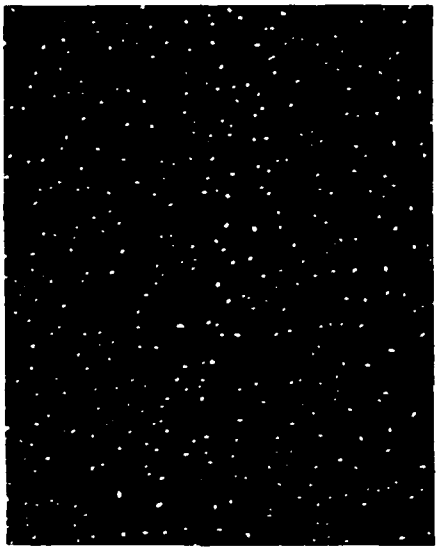


FIG. 1. Quarter section of a Si-$TaSi_2$ eutectic composite transistor is shown in part (a). In this device the source *s* and drain *d* contacts are made with a Au-Sb contact and the gate *g* contact is a $CoSi_2$ film. Part (b), a close-up of the gate ring, shows the size and distribution of the $TaSi_2$ rods.

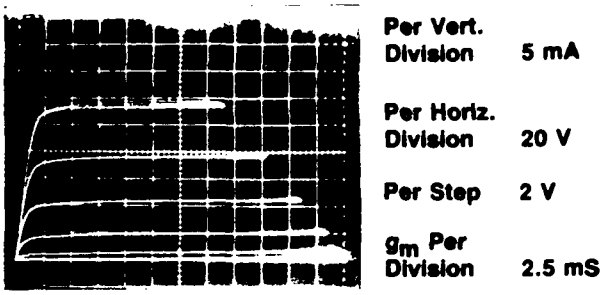
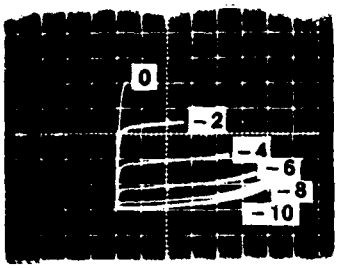


FIG. 2. Characteristics of a Si-$TaSi_2$ eutectic composite transistor. A 10 V reverse bias is required to pinch off the device.

The "pinch-off" condition corresponds to -10 V. This particular wafer had an average interrod spacing of 6.9 μm. Thus for the average 1-μm-diam rod, an average of 4.9 μm of Si matrix separates two rods spaced exactly by the average interrod spacing. With the 10 V pinch-off voltage, the depletion zone around each rod should extend 2.0 μm from each rod/matrix interface. Thus a 10 V bias, leaving 0.9 μm of undepleted Si between channels, should not enable pinch-off. This simple analysis suggests that the pinch-off condition may not be determined solely by the average interrod spacing but by the spacing of the nearest neighbor rods. A similar conclusion was made in a study of the effect of depletion zone size on the composite transport properties.[9]

As illustrated in Fig. 2 the device readily blocks a drain voltage of 240 V. For this carrier concentration, avalanche breakdown is expected at 190 V for a planar one-sided abrupt junction.[10] Thus, the microstructure of this eutectic device is such that it delays avalanche breakdown beyond the expected value for a planar device with a guard ring to minimize junction curvature effects. It was observed that the device failed just above 325 V. Failure was not by avalanche breakdown, but by a catastrophic mechanism that destroyed the device characteristics. Interestingly, the device still functioned if the polarity of the source and drain contacts were reversed. This suggests that the device as originally operated failed in between the gate and drain contacts.

To analyze further the high voltage capabilities of eutectic devices, a 500-μm-thick wafer with a device that failed prematurely at 45 V was thinned to 250 μm and retested with the same polarity. The wafer had a Si matrix carrier concentration of 3×10^{15} cm^{-3}. Surface contacts were arranged in concentric rings as in Fig. 1(a). The width of the gate contact ring was 130 μm (more than six times wider than the device in Fig. 1) and had a smaller gate contact to drain contact spacing of 140 μm. Thinning the wafer resulted in recovery of the device and yielded the characteristics shown in Fig. 3(a). Though leaky at the high drain voltages, the device is shown with a drain voltage of 300 V and with a gate voltage of -10 V. The unbiased curve is cut off at low voltages because a high series resistor was used in the curve tracer to minimize heating effects. This device failed catastrophically when taken to a drain voltage of 325 V. The wafer was thinned further to 125 μm and the device was retested. The characteristics of the same device in the thinner wafer are shown in Fig. 3(b). Again the device recovered and operated with a drain voltage of 600 V. This value is at least three times the blocking voltage of a conventional planar device in a wafer of the same carrier concentration. The high current portions of these characteristics are similarly cut off to avoid heating effects. The saturation current (for the unbiased case) was 27 mA in the 250-μm-thick wafer and 16 mA in the same wafer after thinning. The approxi-



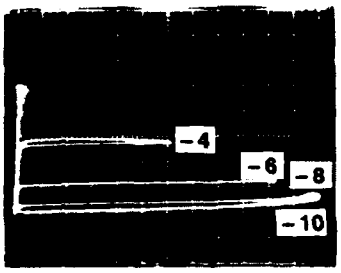
Per Vert. Division 5 mA

Per Horiz. Division 50 V

Per Step 2 V

g_m Per Division 2.5 mS

(a)



Per Vert. Division 2 mA

Per Horiz. Division 50 V

Per Step 2 V

g_m Per Division 1.0 mS

(b)

FIG. 3. Characteristics of the same eutectic composite device tested with a wafer thickness of 250 μm (a) and after thinning to a wafer thickness of 125 μm (b). After taking the device in (a) to 325 V, it failed catastrophically. Thinning the device enabled it to recover and operate at collector voltages as high as 600 V. The low bias voltage cases were not examined to avoid heating effects.

mate proportionality between the current and the thickness verifies that the current channel of the eutectic device is indeed the wafer thickness.

The above experiments suggest that eutectic composite transistors are unusually resistant to avalanche breakdown. None of the many devices fabricated has failed by this mechanism. The mechanism whereby impact ionization is inhibited has not been established yet but it must be related to the interaction of the depletion zone extending outward from the gate rods with the depletion zones around the floating rods between the gate and drain contacts. These floating rods may act to keep the electric field at the gate rods below the critical value for avalanche breakdown. The dependence of the maximum blocking voltage on the wafer thickness is less clear. The polarity and thickness experiments indicate that the device fails when a damage layer is formed at the bottom surface of the wafer between the gate and drain regions. Further analysis is needed to determine the nature of this damage zone.

The potential advantages of these devices stem not only from their high current and voltage switching ability, but also from the simplicity of the device. Due to the presence of closely spaced *in situ* junctions in these wafers, fine line lithography is unnecessary. Also since the Schottky junctions are mostly protected inside the wafer, the devices are less sensitive to contamination. It is also interesting to note the excellent saturation characteristics of these devices, despite a gate structure that is not spaced with lithographic precision. These results may require a better understanding of the importance of uniformly spaced gates in determining device behavior.

In summary, transistor action in a eutectic composite substrate has been demonstrated for the first time. It has been shown that the device has characteristics similar to a MESFET and that the entire thickness of the wafer acts as the current channel. More important, these devices have been shown to be capable of blocking high voltages due to an unusual resistance to avalanche breakdown.

This work was sponsored in part by the Air Force Office of Scientific Research under contract F49620-86-C-0034 and by the Strategic Defense Initiative Office/Innovative Science and Technology (SDIO/IST) and managed by the Office of Naval Research under contract N00014-86-C-0595.

[1]L. A. van Hoof and W. Albers, J. Appl. Phys. **52**, 3476 (1981).
[2]A. S. Yue and J. G. Yu, Proc. Fourth Intl. Conf. Composite Mater., ICCM-IV, Japan Society for Comp. Mater., Tokyo, Japan, 1982, p. 1369.
[3]L. M. Levinson, Appl. Phys. Lett. **21**, 289 (1971).
[4]N. J. Helbren and S. E. R. Hiscocks, J. Mater. Sci. **8**, 1744 (1973).
[5]B. M. Ditchek and M. Levinson, Appl. Phys. Lett. **49**, 1656 (1986).
[6]B. M. Ditchek, B. G. Yacobi, and M. Levinson, Appl. Phys. Lett. **51**, 267 (1987).
[7]B. G. Yacobi and B. M. Ditchek, Appl. Phys. Lett. **50**, 1083 (1987).
[8]M. Levinson, B. M. Ditchek, and B. G. Yacobi, Appl. Phys. Lett. **50**, 1906 (1987).
[9]B. M. Ditchek, B. G. Yacobi, and M. Levinson, J. Appl. Phys. **63**, 1964 (1988).
[10]S. M. Sze, *Physics of Semiconductor Devices* (Wiley, New York, 1969).

END

DATE

FILMED

DTIC

10-88